DLP PRO4500 User's Guide

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About This Guide

The PRO4500 is a next generation DLP module for mini industry projection. This guide is an introductory document that provides an overview of the PRO4500 system and its software. Other documents provide more in-depth information of the hardware and software features of the components of the PRO4500.

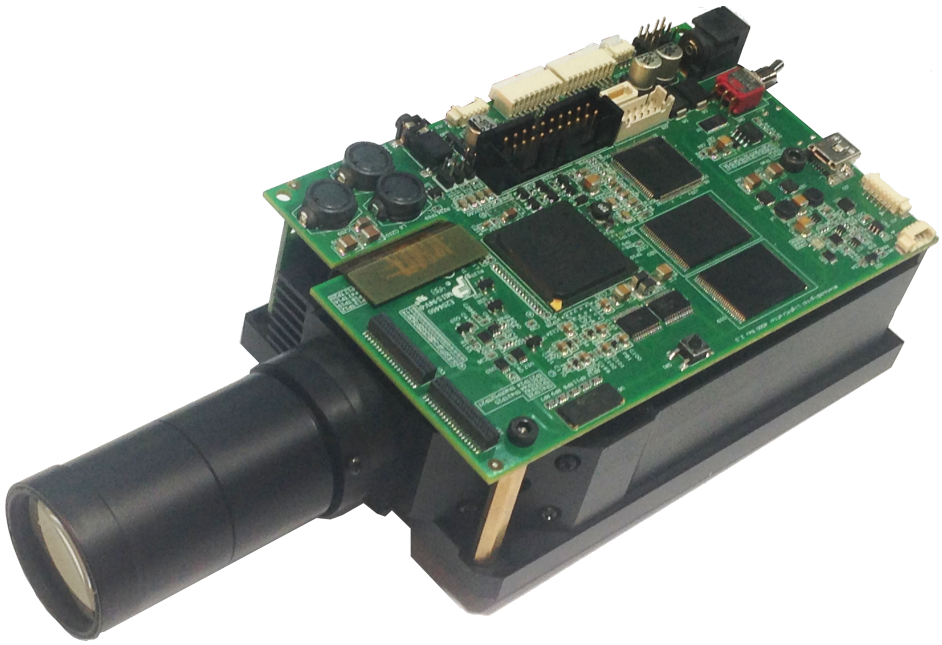

Figure 1. DLP PRO4500 Module

Related Documentation From Texas Instruments
DLPC350 data sheet:DLP Digital Controller for the DLP4500 DMD, DLPS029
DLP4500 data sheet:DLP 0.45 WXGA DMD, DLPS028
DLPC350 and DLP4500 chipset manual:DLP 0.45 WXGA Chipset Data Manual, DLPU009
User's guide:DLPC350 Programmer's Guide, DLPU010

Chapter 1 PRO4500 Overview

1.1 Welcome

This technology brings together a set of components providing an efficient and compelling system solution for:

- Structured light applications:
  - 3D modeling and design
  - Fingerprint identification
  - Face recognition
  - Machine vision and inspection
- Medical and life sciences:
  - Vascular imaging
  - Dental impression scanners
  - Intraoral dental scanners
  - Orthopedics, prosthesis, CT, MRI, and X-ray marking
  - Retail cosmetics
- Small display projectors:
  - Embedded display
  - Interactive display
  - Information overlay

1.2 What is in the PRO4500?

The PRO4500 consists of two subsystems:

- Light engine – includes the optics; red, green, and blue LEDs or UV led; and the 912 × 1140 diamond pixel 0.45- inch WXGA DMD, heat sinks, and fan. The light engine produces approximately 150 lumens (R/G/B led)at 15-W LED power consumption. If use the UV 405nm LED, it can output about 850mw.
- Driver board – includes the LED driver circuits, DLPC350 DMD controller, power-management circuits, DVI-to-RGB conversion with the TFP401, and a 32-MB flash storage

Figure 1-1 shows the major hardware components.

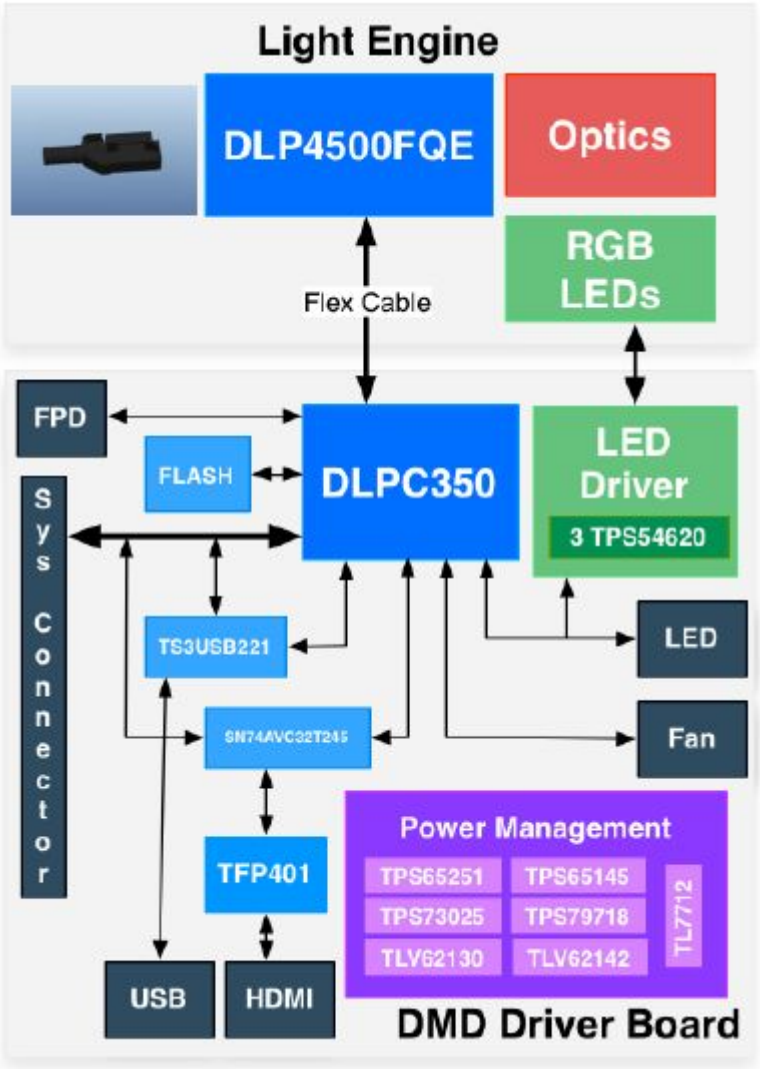

Figure 1-1. PRO4500 Block Diagram

1.2.1 Light Engine

Wintechdigital developed the PRO4500 Light Engine. As shown in Figure 1-2, the light engine includes:

- DLP4500FQE or FQD DMD
- DMD heat sink
- Red, green, and blue LEDs or UV LED.
- Focus control
- Uniformity illumination system.
- Projection lens

The Light Engine is mounted on top of a large thermal plate to cool the module. The DLP4500 DMD is mounted vertically between the DMD heat sink and the light engine. On the side same to the DMD, the red and green LEDs are mounted between a thermal plate and the light engine. The blue LED is mounted between a thermal plate and the light engine, next to the

opposite side of projection lens. An LED heat sink is mounted behind the red and green LED thermal plate and thermally connected to the blue LED thermal plate. A fan forces air across the LED heat sink to cool the LEDs. The light engine,not including the LED heat sinks, has a length of 200 mm, width of 72 mm, and height of 26 mm.

Feature:

1 All the lens are made with glasses, no any plastic lens.
2 All the mech parts are made with metal.
3 0% offset optics.
4 compatible with s241 and s310 DMD.
5 accept numerous field of view and working distance projection lenses.
6 swappable projection lenses.
7 various LED compatibility.

Table 1-1. Light Engine Specifications

Parameter	Min	Typ	Max	Unit
Output power	700	850	1100	mw
Uniformity	94		105%	%
Contrast(full on/full off)	700:1			
F-number	2.4			
Throw ratio	See table 2			
Offset	0			%
FOV	See table 2			

Working distance	Source	wavelength	offset	Throw ratio	Focus range	FOV	畸变
92	LED	405±10nm	0%	1.4	About 10mm	65.6mmX41mm	<0.8%
184	LED	405±10nm	0%	1.4	About 50mm	131.2mmX82mm	<0.8%
119	LED	405±40nm	0%	2.3	About 8mm	51.6mmx32.2mm	<0.1%
700	LED	450-660	0%	1.82	About 1000mm	384mmX240mm	<0.1%

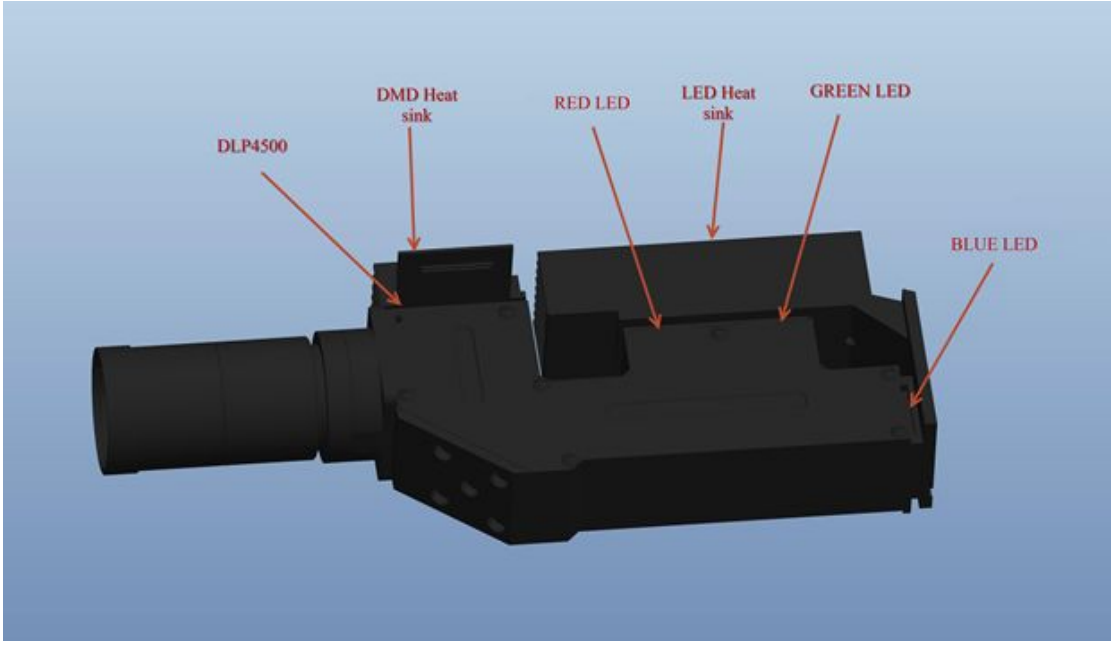

Figure 1-2. Light Engine

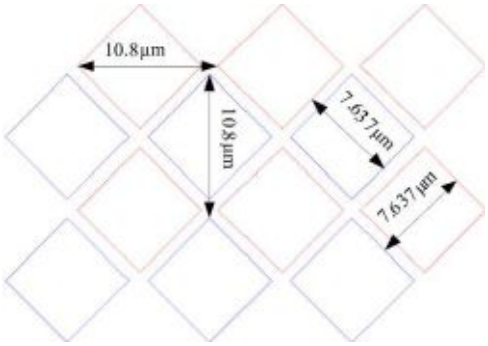

Figure 1-3. 0.45-Inch DMD Diamond Pixel Geometry

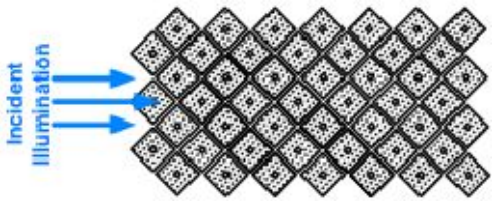

Figure 1-4. 0.45-Inch DMD Diamond Pixel Array Configuration

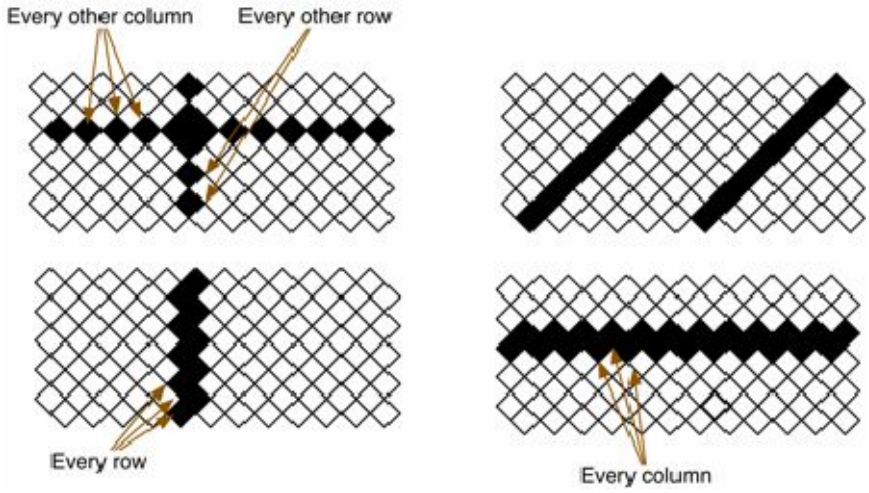

Figure 1-5. Diamond Pixel for Vertical, Horizontal, and Diagonal Lines

1.2.1.1 Light Engine Thermal Limits

The PRO4500 is an actively cooled system with a thermal limit requiring that of all three simultaneous LED currents is less than 4.3 A.

CAUTION
Do not overheat the system by driving all LEDs at maximum power.

1.2.2 Driver Board

The PRO4500 driver board contains the electronics to drive the DLP4500 DMD, LEDs of the light engine, and the LED cooling fan. The driver board offers several interface options for USB, I2C, trigger inputs and outputs, video input through mini-HDMI and FPD-link connector, and a system board interface. Figure 1-6 shows the driver board block diagram of the PRO4500.

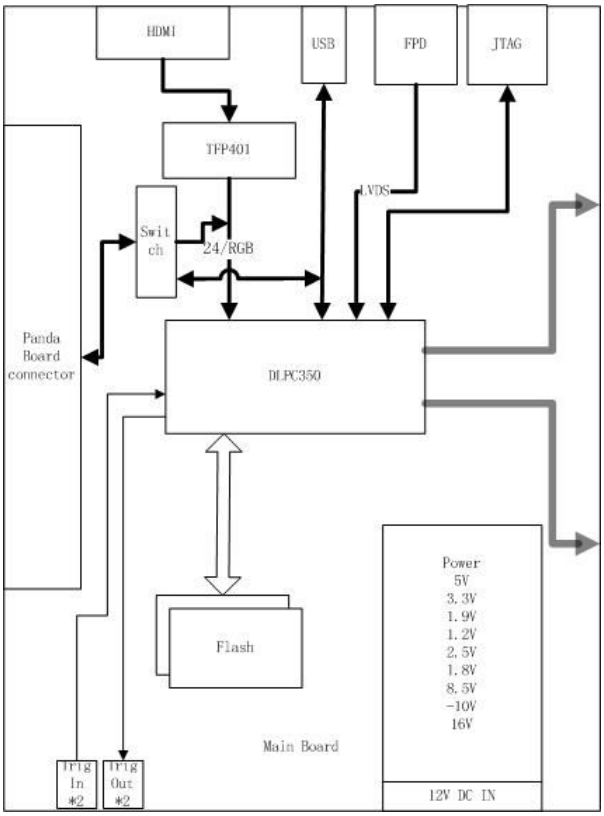

Figure 1-6. PRO4500 Driver Board Block Diagram

The PRO4500 driver board major components are:

- DLP4500: 0.45 inch-WXGA DMD
- DLPC350: DLP4500 controller
- 32-MB parallel flash contains DLPC350 firmware and 24-bit compressed images
- Power management:

– TPS65251: Triple output buck switcher for DLPC350 1.2-V, 1.9-V supplies and 5-V board supply.
– TPS65145: Triple output boost converter for DLP4500 8.5-, –10-, and 16-V supplies
– TPS73025: Step-down converter for DLP4500 2.5-V supply
– TLV62130: Step-down converter for 3.3-V supply
– TLV62130: Step-down converter for 5-V system board supply
– TPS79718: LDO for DLPC350 1.8-V analog supply
– TL7712: Programmable time delay for power-supply sequencing
TFP401: Digital Receiver for DVI to 24-bit parallel RGB interface
TS3USB2221A: ESD-protected high-speed USB multiplexer
SN74AVC32T245: 32-bit dual supply bus transceiver for system board interface

1.2.3 System Board

The PRO4500 driver board allows the connection of a Wintechdigital's ELC4460. See, Chapter 6.

1.3 PRO4500 Connections

Figure 1-7 and Figure 1-8 depict the switches and connectors with their respective locations. The following list corresponds to the callouts on these figures. The figure does not include cables, or a power supply.

1. Reset button
2. Power connector: Use a power supply with a 12-V DC output with current of 6 to 7-A rating and a plug of 2.5-mm inner diameter × 5.5-mm outer diameter and 9.5-mm female center positive shaft. The current output of the power supply determines how much current the LED driver can supply
3. External trigger output connector: Supports two trigger output signals, each with configurable voltage of 3.3 V and 1.8 V through jumpers, J13 and J15, respectively.
4. Mini-USB connector: use an A to mini-B USB cable to connect to a PC.
5. UART/RS232 mini-plug connector output: DLPC350 3.3-V UART output for error messages. Mini-plug tip is DLPC350 transmit (TX) and ring is DLPC350 receive (RX) signals. UART has the following serial configuration: (Not installed)
   - Bits per second: 115200
   - Data bits: 8
   - Parity: None
   - Stop bits: 1
   - Flow control: None
6. External trigger Input connector: Supports two trigger input signals, each with configurable voltage of 5 V, 3.3 V and 1.8 V through jumpers, J10 and J12
7. Stand-by switch: Places the PRO4500 in standby mode, powering down the LED driver and the DLPC350 (Not installed)
8. Flat panel display-link connector(Not installed)
9. Fan connector
10. LED driver power connector
11. LED driver control connector
12. DLPC350 I2C1 bus
13. DLPC350 I2C0 bus
14. External LED driver connector: Install a jumper in J30 to disable the PRO4500 LED drivers and set jumper J28 for 3.3-V or 1.8-V supply. Then use this connector to control an external LED driver board to power the LEDs of the PRO4500 light engine or external light engine.
15. System board connector: This interface routes USB, I 2 C, GPIO, and triggers from DLPC350 to a system board to control the PRO4500.
16. Light engine connector control
17. JTAG connector for DLPC350
18. JTAG Boundary Scan for DLPC350 (bottom of the board) (Not installed)
19. DVI input through mini-HDMI connector (bottom of the board). This input supports resolutions of 1280 × 800, 1024 × 768, 1024 × 640, 912 × 1140, 800 × 600, 800 × 500, and 640 × 480 at up to 120 Hz. In Video Mode, the DLPC350 scales the input resolution to the native resolution of the DLP4500 DMD. In Pattern Sequence mode, this

input supports 912 × 1140 resolution.

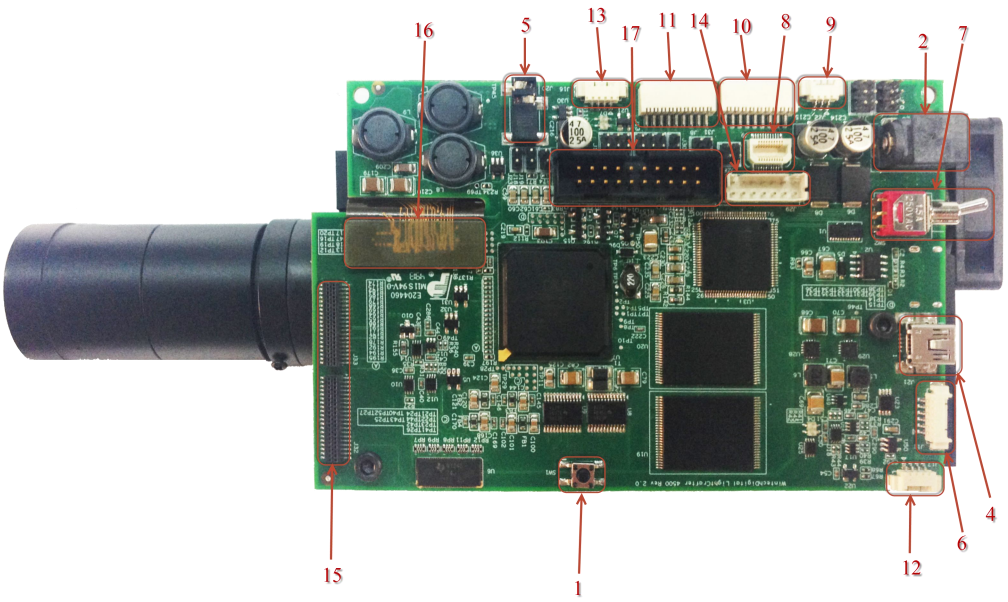

Figure 1-7. PRO4500 Connectors (Top View)

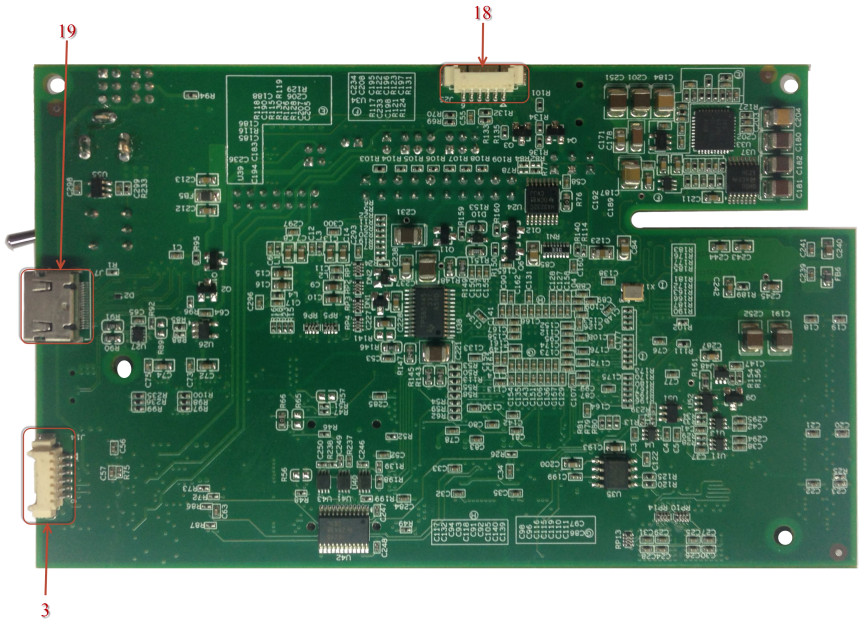

Figure 1-8. PRO4500 Connectors (Bottom View)

1.4 PRO4500 Jumpers

The PRO4500 has jumper options to disable the onboard LED driver, control voltages of the LED signals to an external board, and control the trigger input and output voltages. This section lists all the jumpers on the PRO4500 driver board. Figure 1-9 depicts the locations of these jumpers. These jumpers require a 2-mm jumper, like Sullins Connector Solutions ® SPN02SYBN-RC, Digi-Key part number S3404-ND.

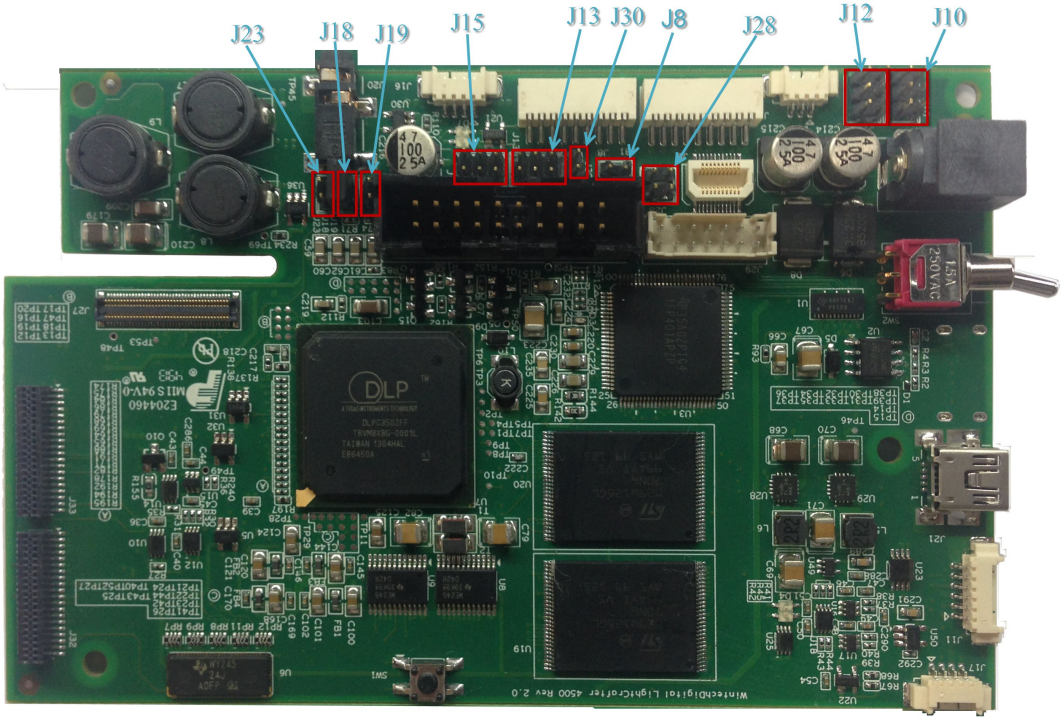

Figure 1-9. PRO4500 Jumper Locations

J8: EDID write protect disable jumper. Place this jumper to reprogram the EDID EEPROM (U2) using I2C commands through the mini-HDMI connector. Remove the jumper when programming of the EDID is complete. The EDID is programmed at the factory with resolutions of 1280 x 800 and 912 x 1140.

J10: DLPC350 TRIG1_IN voltage selection. See to Figure 1-10.

- Jump across pins 5 to 6 for 5 V
- Jump across pins 3 to 4 for 3.3 V
- Jump across pins 5 to 6 for 1.8 V

J12: DLPC350 TRIG2_IN voltage selection. See to Figure 1-10.

- Jump across pins 5 to 6 for 5 V
- Jump across pins 3 to 4 for 3.3 V
- Jump across pins 5 to 6 for 1.8 V

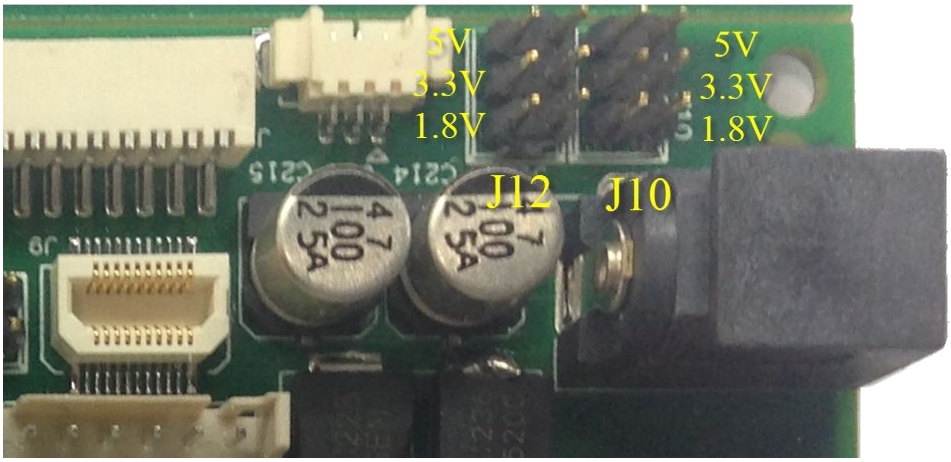

Figure 1-10. PRO4500 J10 and J12 Voltage Jumpers

J13: DLPC350 TRIG1_OUT voltage selection. See to Figure 1-11.

- Jump across pins 5 to 6 for 5 V
- Jump across pins 3 to 4 for 3.3 V
- Jump across pins 5 to 6 for 1.8 V

J15: DLPC350 TRIG2_OUT voltage selection. See to Figure 1-11.

- Jump across pins 5 to 6 for 5 V
- Jump across pins 3 to 4 for 3.3 V
- Jump across pins 5 to 6 for 1.8 V

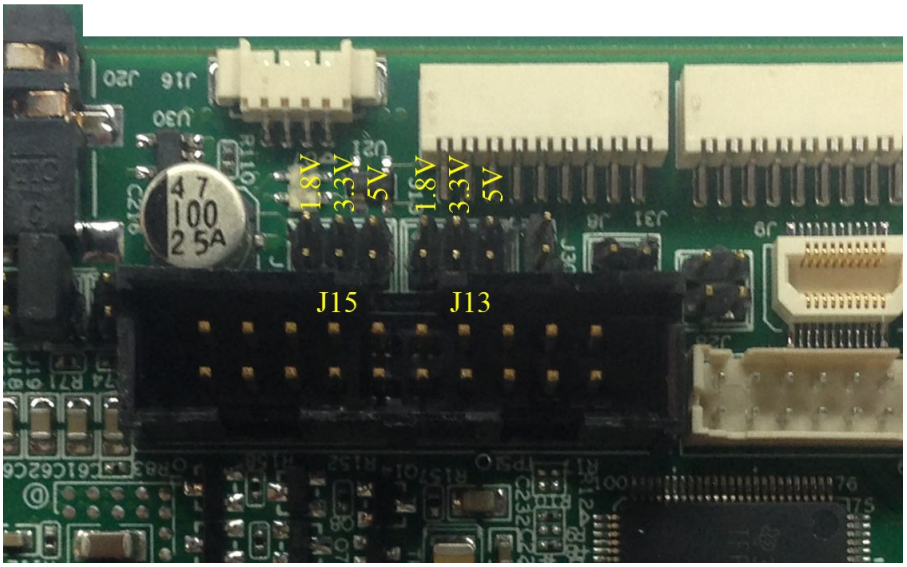

Figure 1-11. PRO4500 J13 and J15 Voltage Jumpers

J18: DLPC350 HOLD_IN_BOOT. Jump across this header to hold the DLPC350 in bootloader mode. This action is needed only if the PRO4500 firmware becomes corrupted and must be reprogrammed through the JTAG boundary scan or USB. The graphical user interface (GUI) firmware upgrade process places the DLPC350 in bootloader mode through software commands and does not need the jumper.

J19: Device address select

- Jump across header to set I 2 C address to 0x3A and USB device serial number to LCR2.
- Do not populate jumper to set I 2 C address to 0x34 and USB device serial number to LCR2.

J23: Hold in reset. Jump across header to drive and hold reset line low. Jumping across this header is equivalent to pressing and holding the reset switch.

J28: DLPC350 LED signals voltage selection. This jumper must be populated when bypassing the onboard LED driver and using an external LED driver.

- Jump across pins 1 to 2 to set the DLPC350 LED enables and PWM signals to 3.3 V.
- Jump across pins 3 to 4 to set the DLPC350 LED enables and PWM signals to 1.8 V.

J30: DLPC350 LED driver disable. This jumper must be populated when bypassing the onboard LED driver and using an external LED driver.

- Jump across header to disable the onboard LED driver and turn off all LEDs, regardless of the DLP PRO4500 video mode.
- Do not populate this header for normal operation using the onboard LED driver.

1.5 Dimensions

The PRO4500 optical engine is mounted on top of a thermal plate to provide passive cooling to the module. A heat sink and fan provide active cooling to the LEDs. The DLP4500, 0.45-in. DMD, is vertically mounted at the end of the optical engine and attached with a flex cable to the driver board that lies on top of the light engine. The dimensions of the PRO4500 are of 98 mm long, 121.6 mm wide, and 47.7 mm tall. Figure 1-12 shows PRO4500 dimensions.

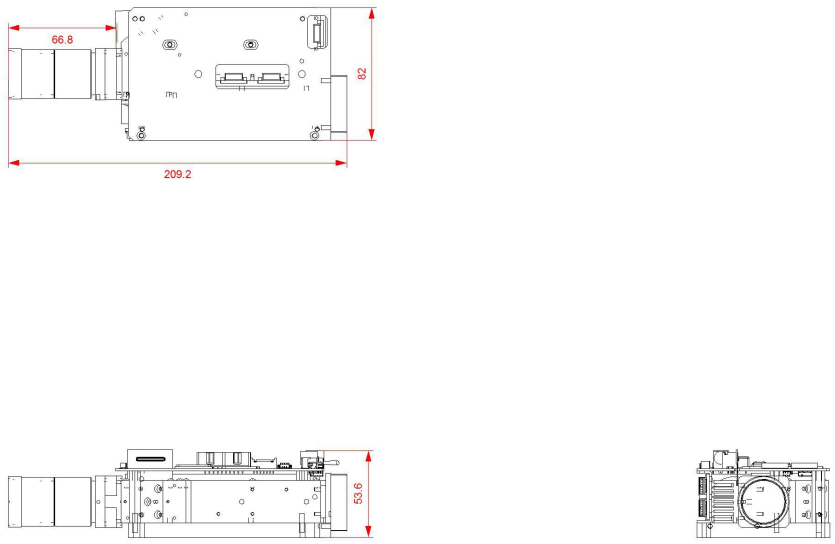

Figure 1-12. PRO4500 Dimensions

Chapter 2 Quick Start

This chapter details the steps to power up the PRO4500 and connect to a PC.

2.1 Power-up the PRO4500

The PRO4500 is ready to use, out of the box. Steps 1 through 5 show how to power, display an image, and connect the device to a PC.

1. Connect a 12-V DC power supply to the power supply connector (connector 2 in Figure 1-8).
2. An LED on the top of the PRO4500 board, D4 lights up green. The fan starts, stops, and then restarts while the DLPC350 is booting. After 5 to 10 seconds, the DLPC350 bootloads and displays a screen with the DLP and PRO4500 logo. The D4 LED on top of the PRO4500 board flashes on and off green. If the board shuts down after briefly turning on the display, the power supply current rating might be too low.
3. To display video, connect a DVI source to the mini-HDMI connector (connector 20 in Figure 1-8).
4. Control the PRO4500 with the free GUI software (available to download from http://www.ti.com/dlplightcrafter4500).
5. After installing the software on the computer, connect the PC to the PRO4500 using a USB to mini-USB cable (connector 4 in Figure 1-8). The first time the cable is connected on a PC, ThePRO4500 emulates a USB composite device with human-interface device (HID) class. No drivers are required because these drivers are natively handled by all operating systems.

Chapter 3 Operating the PRO4500

This chapter introduces the PC software provided with the PRO4500.

3.1 PRO4500 Software

The PRO4500 includes a QT-based GUI application to control the module through the USB interface. QT is a Nokia cross-platform application and user-interface framework with open source and commercial licenses. To install the QT GUI, just expand the LightCrafter4500_GUI.zip file into a directory and double-click on the executable file.
The PRO4500 supports two main modes of operation:

•Video mode displays images from:
– DVI input through the mini-HDMI connector
– 24-bit RGB bitmaps stored in flash memory
– 24, 20, 16, 10, and 8-bit RGB input through the system board connectors (J1, J3, J4, and J6)
– Internal test patterns
– 30-bit RGB through flat panel display (FPD) link

•Pattern Sequence mode displays images from:
– 1-, 2-, 3-, 4-, 5-, 6-,7-, and 8-bit bitmap images stored in flash memory
– 1-, 2-, 3-, 4-, 5-, 6-, 7-, and 8-bit bitmap images streamed through the DLPC350 24-bit RGB interface (mini-HDMI, FPD-link, or system board connectors)

3.2 PC Software

Upon execution of the LightCrafter4500.exe file, the window shown in Figure 3-1 displays. The GUI window contains the following two sections:
• The top portion of the GUI window displays the System Control and controls the Operating Mode, Image Orientation,LED Driver Control settings, and LED Selection. There are also controls for saving and applying solutions.
• The bottom portion of the GUI window offers a set of tabs to further control the selected Operating Mode.

In any of the GUI sections, clicking a Get button reads the current settings of that particular subsection. Clicking the Set button programs the settings in the respective subsection. Some commands may require additional steps before the GUI display is updated.

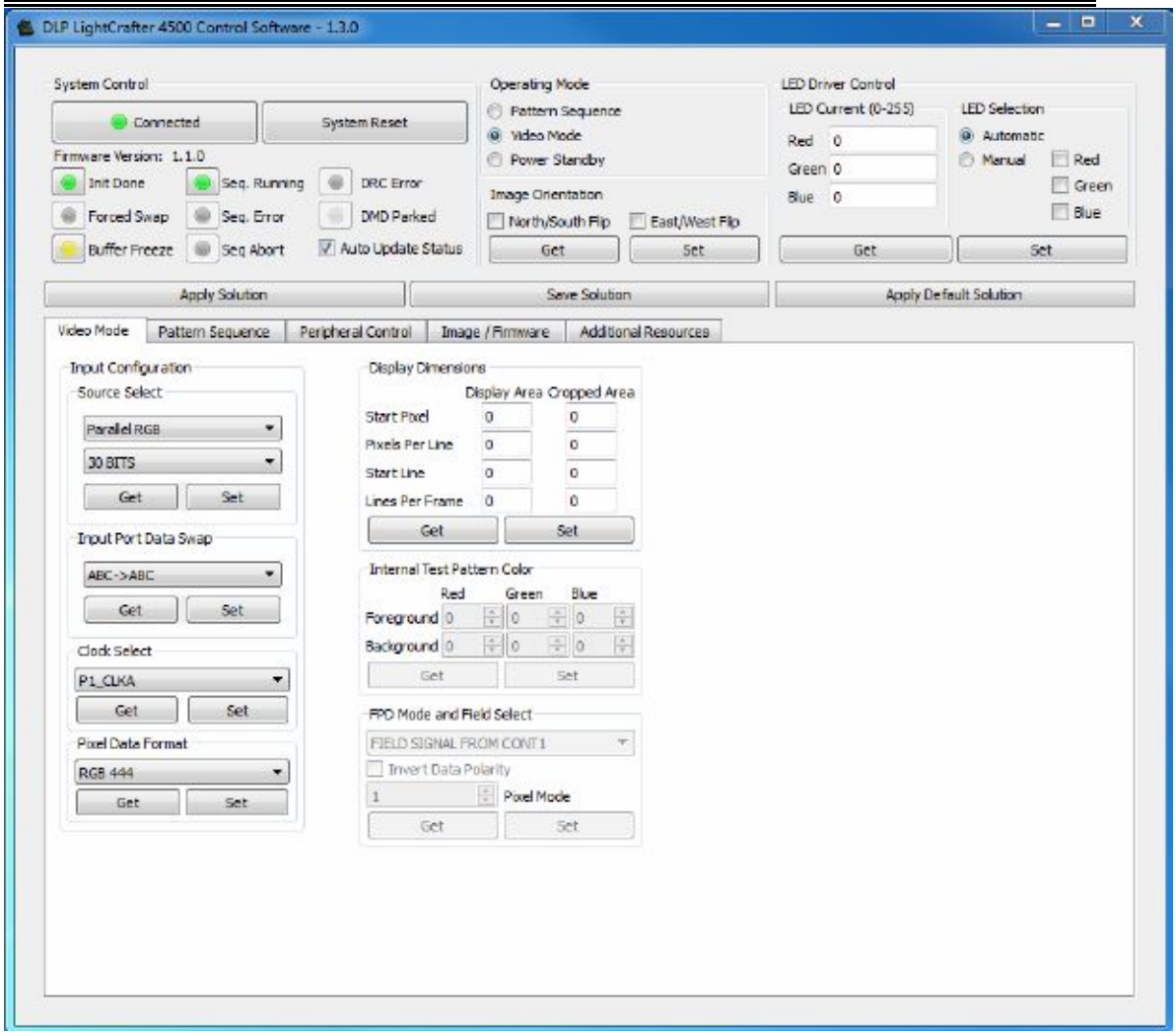

Figure 3-1. PRO4500 GUI – Video Mode

The PRO4500 GUI communicates with the DLPC350 using USB 1.1. The DLPC350 emulates as a USB device with HID support. The PC polls all the HID peripherals and once the PC detects the DLPC350, the Connected button changes to green. If the USB cable is disconnected, the color of the Connected button changes to red and the Connected text is grayed-out. Once the System Status shows Connected, the firmware version, hardware, and System Status indicators are displayed. There is no need to press the Connected button, because the HID peripheral is detected by the operating system after USB enumeration.

3.2.1 System Status

At the top-left portion of the GUI window, the hardware and System Status indicators report the following:

- Init Done: When highlighted green, it indicates the successful completion of the DLPC350 initialization. When highlighted grey, it indicates the DLPC350 had an error during initialization.

- Sequencer Running: When highlighted green, the DLPC350 sequencer is running as usual. When highlighted gray, the DLPC350 sequencer is stopped.
- DRC Error: DMD Reset Controller Error indicator. When highlighted grey, the DMD Reset Controller has not detected an error. When highlighted red, the DMD Reset Controller has found multiple overlapping bias or reset operations accessing the same DMD block of micromirrors.
- Forced Swap: When highlighted red, the DLPC350 sequencer detected a forced buffer swap error indicating that image data has been displayed from the wrong internal display buffer. When highlighted gray, no buffer swap error has occurred. This error can occur if the PRO4500 is set to Video Mode and the vertical backporch timing is too small. The error can also occur if the DLP PRO4500 is set to Pattern Sequence mode with patterns input from the video port and pattern sequence timings do not match the video port VSYNC.
- Sequencer Error: When highlighted red, the DLPC350 sequencer has detected an error. When highlighted gray, the DLPC350 sequencer detected that no error occurred.
- DMD Parked: When highlighted yellow, the DMD micromirrors are parked in the position normal to the DMD plane. When highlighted gray, the DMD micromirrors are not parked.
- Buffer Freeze: When highlighted yellow, the frame buffer is frozen. When highlighted gray, the frame buffer is not frozen. This is cleared on the next buffer swap.
- Sequencer Abort: When highlighted red, the DLPC350 sequencer has detected an error condition that caused an abort. When highlighted gray, the DLPC350 sequencer detected that no error occurred.

These indicators are updated every 2 seconds, or when a command is issued to the DLPC350.

- Auto Update Status. When checked, all indicators will continue to update every two seconds. When unchecked, the indicators will stop updating and turn gray. While running in Pattern Sequence Mode, keeping the option unchecked prevents the GUI from interrupting the DLPC350 controller which will be processing critical functions related to pattern display.

3.2.2 Operating Mode

To the right of the System Status, the Operating Mode sets how the PRO4500 operates:

- Video Mode: The DLPC350 takes 24, 20, 16, 10, and 8-bit data from one of the following interfaces:
  - 24-bit RGB interface
  - FPD-link interface
  - Internal test pattern generator
  - Flash memory

The DLPC350 then applies video processing functions, such as scaling, gamma

correction, and color coordinate adjustments, and sends the processed image to the DMD.

- Pattern Sequence mode: The DLPC350 takes 1-, 2-, 3-, 4-, 5-, 6-, 7-, and 8-bit data from one of the following interfaces:
  - 24-bit RGB interface
  - FPD-link interface
  - Flash memory

The DLPC350 does not apply any video processing functions and provides a pixel accurate mode where every pixel maps to the native DMD resolution of 912 × 1140.

- Power Standby: Places the DLPC350 in low-power state and powers down the DMD interface.

3.2.3 Image Orientation

Beneath Operating Mode, the Image Orientation controls the long and short axis flips to support front, rear, table, and ceiling mounted projection. The Image Orientation occurs on the next image or frame load in Video mode, and on the next download to the PRO4500 in Pattern Sequence mode.

• East/West Flip: If checked, the image is flipped along the east and west axis of the projected image.

Usual table front projection has this setting unchecked. Otherwise, the image is flipped horizontally.

•North/South Flip: If checked, the image is flipped along the north and south axis of the projected image. Usual table front projection has this setting unchecked. Otherwise, the image is flipped vertically.

3.2.4 LED Current Settings

On the top-right of the GUI window, the LED Current settings control the individual currents of the red, green, and blue LEDs. A setting of 255 corresponds to the maximum LED current. A setting of 0 corresponds to minimum LED current.

Typical variations in LED manufacturing can lead to changes in the brightness and current consumption.

Thus for typical white balance point, TI recommends the following percentages of colors:

Red or green is approximately 87.5%

Blue or green is approximately 97.6%

At the default LED current values of:

Red = 104

Green = 135

Blue = 130

The LED Selection box determines the control of the LED enables signals. Two options are allowed:

•Automatic: LED enables are controlled by the DLPC350 sequencer. In Video Mode, the

LED enables are set in color sequential order. In Pattern Sequence mode, the LED enables are controlled by the downloaded Pattern Sequence settings.

•Manual: LED enables are controlled by the check boxes. Checking a color, continuously enables the LED of that color at the given LED current setting.

3.2.5 Video Mode

When the PRO4500 is configured in Video Mode, the Input Source Select section in Figure 3-1 in the top-left part of the Video Mode tab selects the input source to be displayed by the DLPC350. The DLPC350 treats these as video inputs and applies image processing functions, like scaling, gamma correction, color coordinate adjustments, and so forth. The following lists the allowable input sources:

• Parallel RGB interface: Supports 24-, 20-, 16-, 10-, and 8-bit data inputs. This interface is connected to the TFP401 for DVI input from the mini-HDMI connector or to the system board connectors. The Pixel Data Format section is below the Source Select interface selects the allowable pixel data formats for the Parallel RGB interface:

– RGB 4:4:4
– YCrCb 4:4:4
– YCrCb 4:2:2

• Internal Test Pattern: 24-bit internal pattern generator with RGB 4:4:4 pixel data format. The internal test patterns offer color control of the foreground and background color of the pattern through the Internal Test Pattern Color section. The available internal test patterns and their respective foreground and background color control are:

– Solid field: Foreground color control only
– Horizontal ramp: Foreground color control only
– Vertical ramp: Foreground color control only
– Horizontal lines: Foreground and Background color control
– Diagonal lines: Foreground and Background color control
– Vertical lines: Foreground and Background color control
– Grid: Foreground and Background color control
– Checkerboard: Foreground and Background color control
– Red, green, and blue ramps: Foreground color control only
– Color bar: Foreground color control only
– Step bar: Foreground color control only

• Flash images: single-frame, 24-bit Still images stored in external flash memory. The flash memory supports up to 32MB of storage with up to 64 images. The images stored in flash memory support RGB 4:4:4 and YCrCb 4:2:2 pixel data formats.

• FPD-link: Flat Panel Display Link connector. The FPD-link interface supports 30-, 24-, 20-, 16-, 10-, and 8-bit data inputs with RGB 4:4:4 pixel data format. The FPD Mode and Field Select configures the mapping of the pixel mode, polarity, and CONT1 and CONT2 field signals.

For the Parallel RGB and FPD-link video input modes, the DLPC350 interprets channel A as green, channel B as red, and channel C as blue. However, the Parallel RGB or

FPD-link source can have different mapping of channels to colors. The Input Source Port Data Swap section sets the mapping of channels to colors. Port1 refers to Parallel RGB interface while Port2 refers to the FPD-link interface. The mapping options are:

- ABC→ABC, no swapping of data subchannels
- ABC→CAB, data subchannels are right-shifted and circularly rotated
- ABC→BCA, data subchannels are left-shifted and circularly rotated
- ABC→ACB, data subchannels B and C are swapped
- ABC→BAC, data subchannels A and B are swapped
- ABC→CBA, data subchannels A and C are swapped

For all video input modes, the Display Dimensions section defines the active displayed resolution. The maximum supported input and output resolutions for the DLP4500 0.45 WXGA DMD are 1280 pixels (columns) by 800 lines (rows). The display area settings set the first pixel column (Start Pixel) and the first line (Start Line) as well as, the numbers of pixels per line (total columns) and the number of lines per frame (total rows). This setting also provides the option to define a subset of active input frame data using pixel (column) and line (row) counts. In other words, this feature allows cropping of the source image as the first step in the processing chain.

3.3 Pattern Sequence Mode

When the PRO4500 is configured in Pattern Sequence mode, the DLPC350 supports 1-, 2-, 3-, 4-, 5-, 6-, 7-, and 8-bit images with a 912 columns × 1140 rows resolution. These images are pixel accurate, meaning that each pixel corresponds to a micromirror on the DMD and is not processed by any of the video processing functions. Three subtabs control the Pattern Sequence settings:Sequence Settings,Trigger Controls, and LED Delay Control.

3.3.1 Sequence Settings

A pattern sequence is composed of several patterns loaded from flash memory or streamed through the 24-bit RGB video port. Each individual pattern can have a specific set of LEDs illuminating it, a particular bit-depth, and an internal or external trigger. The Sequence Settings subtab lets the user define and set all the Individual Pattern Settings. The Trigger Controls subtab and the LED Delay Control subtab set the trigger and LED enable edge timings, respectively. Figure 3-5 shows the PRO4500 GUI with the Pattern Sequence tab selected.

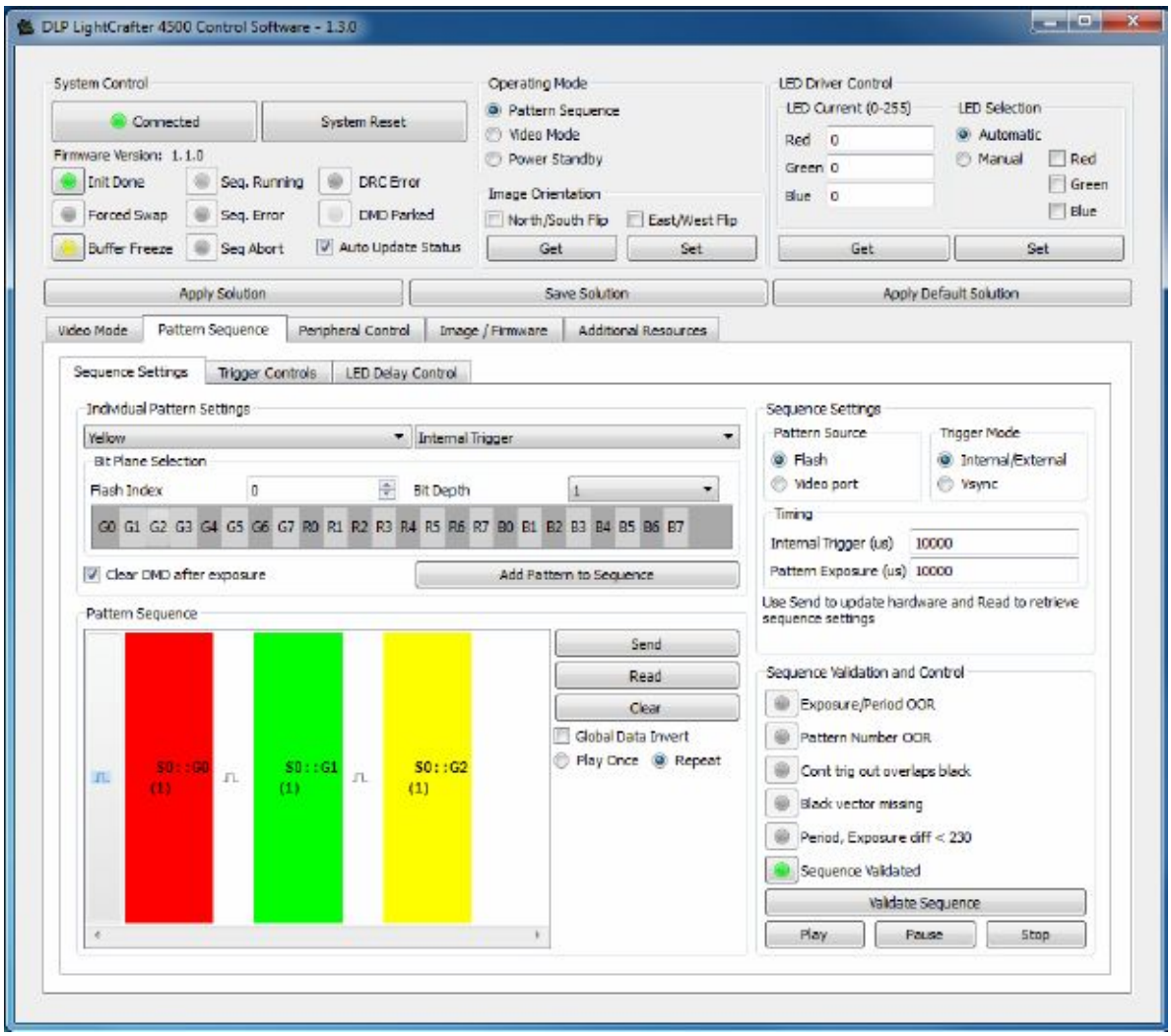

Figure 3-5. PRO4500 GUI – Pattern Sequence Mode

The Pattern Sequence displays images from one of the following two input sources:

- Flash: Images stored in flash memory. The flash memory can store up to sixty-four 24-bit compressed images.
- Video port: Streamed through the Parallel RGB or FPD-link interface. Only one of these interfaces can be connected to the PRO4500 during Pattern Sequence mode.

To synchronize a camera or external system with the displayed patterns, the PRO4500 supports a set of trigger inputs and outputs. These inputs and outputs are configured through the Trigger Mode section and Trigger Controls subtab. The Trigger Mode selects the trigger input:

- Internal/External: Uses an internal trigger period to start the pattern sequence or uses the DLP PRO4500 TRIG_IN2 signal to start and pause the pattern sequence. Each pattern in the pattern sequence can be configured with either an internal or external trigger. With the Internal Trigger setting, the Internal Trigger Period displays the next pattern. With External Trigger Period, the DLP PRO4500 TRIG_IN_1 signal displays

the next pattern.

- Vsync: Uses the VSYNC signal from the Parallel RGB or FPD-link interface to trigger the start of the pattern sequence. After VSYNC, the patterns are displayed in the sequence shown on the Pattern Sequence section. Each pattern length is determined by the Pattern Exposure time. Thus, the total number of patterns multiplied by the pattern exposure must be less than or equal to the VSYNC period.

Pattern sequence timing is controlled by the Internal Trigger period and Pattern Exposure period.

Depending on the setting of the Pattern Source section, the bottom field will toggle from Image Load Time and Vsync period if the Pattern Source is set to flash images or video port, respectively.

• Internal Trigger period: Defines the amount of time between patterns (in microseconds) in a pattern sequence.

• Pattern Exposure period: Defines the amount of time a single pattern is displayed in microseconds.

• Vsync period: Only applicable when Pattern Source→Video port is selected. This field defines the amount of time between VSYNC pulses in microseconds. This field is used to validate the data programmed to the PRO4500 and must match the VSYNC period of the Video interface (Parallel RGB or FPD-link).

• Image Load Time: The time it takes to load 24-bit fields of an image from external flash memory. Typical time is 200 ms. Once an image is loaded from flash, 24 bit-fields reside in the frame buffer and can be sequenced at higher speeds. Two 24-bit field display buffers are available in the DLPC350. If the pattern sequence uses more than two images (48-bit fields), then approximately 200 ms is required to load the new image into the DLPC350 internal display buffer.

A pattern sequence can be any combination of bit depth patterns with any combination of LED sources. The pattern sequence can be played once or continuously repeated. The allowed LED sources are:

• White: Red, green, and blue LEDs on
• Cyan: Green and blue LEDs on
• Magenta: Red and blue LEDs on
• Yellow: Red and green LEDs on
• Red: Only red LED on
• Green: Only green LED on
• Blue: Only blue LED on

To create a pattern sequence, follow these steps:

1. Choose pattern input source (Flash or Video port) from the Pattern Source section.
2. Choose internal or external, or VSYNC trigger mode from the Trigger Mode section.
3. Set the appropriate Trigger Controls,see Section 3.3.2
4. Set the Internal Trigger period, Pattern Exposure period, and Image Load Time or Vsync Time.
5. If the patterns sequence must be played once, set Play Once in Figure 3-5. This setting will play the number of patterns set in Trigger Controls subtab under "Trigger 2

Patterns per pulse". If set to 1, it plays the first pattern in the sequence and stops. If set to 10, it plays the first 10 patterns in the sequence. If the pattern sequence is to continuously repeat, set repeat. Make sure to click the Send button after clicking on Play Once to download the new settings.

6. Create the pattern sequence:
   (a) Choose the flash Image Index and set the bit depth on the Individual Pattern Settings.Note: if input from Splash Image) or Frame index clarified things about video port sourced pattern sequence(if input is from video port, this frame index are the RGB 0-7 you see in the box below. In pattern sequence mode, you are not sending a standard 24 bit RGB image, you are sending a group of images in parallel, anywhere from 3 8-bit images (grayscale) to 24 individual 1-bit images. The color is determined by the LEDs. Then select the desired bit-plane to be displayed. The bit-planes are labeled G0+G7, R0+R7, and B0+B7. Clicking on these squares will select this bit-plane. When the source is the video port, the trigger will always be VSYNC, be sure to set the VSYNC period to be equal to that of your display (i.e. The next pattern in the sequence you construct will display each v_sync).Note that if using the video port, the incoming image resolution must be 912x1140
   (b) Choose the LEDs to illuminate this bit-plane
   (c) Select the trigger for the pattern: no trigger, external positive, external negative, or internal trigger. "Internal trigger" has an internal hardware signal that goes as input to the pattern display state machine (meaning the controller starts displaying after receiving the signal), whereas the "no internal trigger" option will display a pattern without waiting for a trigger; each pattern will display in continuation with the previous pattern. Creating an internally triggered pattern sequence with an external trigger input may cause unexpected behavior.
   (d) If a black image is desired between patterns, check the Clear DMD after exposure.
   (e) Click the Add Pattern to Sequence button.
   (f) Repeat Steps A through E to for each pattern in the sequence.
7. Click Send to LightCrafter. This executes a data validation and provides results in the Data Validation status section and informs the user if any of the trigger period or exposure are invalid. After successful data validation, the pattern sequence is downloaded to the PRO4500 and started.

If a data validation problem occurs, the appropriate status indicators are highlighted in the Data Validation section:

- Exposure/Period OOR: When highlighted red, the Pattern Exposure period or Frame period is out of range. The pattern exposure period must be greater than the fastest period supported, as listed in Table 4-1.
- Pattern Number OOR: When highlighted red, the Pattern Number is out of range. The maximum allowed patterns depend on the bit width and are listed in Table 4-1.
- Cont trig out overlaps black: When highlighted red, the continuous pattern exposure has a trigger Out1 request or overlapping black sectors.

- Black vector missing: When highlighted red, the black vector is missing (this may also be referred to as the "post vector").
- Period, Exposure diff < 230: When highlighted red, the difference between the frame period or internal trigger period and the exposure period of a pattern is less than 230 µs. The DMD needs 230 µs for load a pattern, so the trigger or frame period must be 230 µs greater than the pattern exposure time.

Pause or restart the pattern sequence through the Pause and Play buttons, respectively. If a pattern sequence was previously loaded, the user can click the Read button to load the sequence into the GUI window.

The Pattern Sequence section shows the pattern sequence as a set of colored rectangles. The color corresponds to the LEDs used. The entries on the rectangles represent the image source, the bit-plane, and the bit-depth as follows: S0::G0 (1) indicates flash location 0, bit-plane = G0, bit-depth = 1. F2::G5 (3) indicates Frame 2, bit-plane = G5, bit-depth = 3. For example, in Figure 3-5, a pattern sequence of three patterns is displayed. Each pattern is triggered every 100 ms and exposed for 100 ms. The first pattern is a 1-bit green pattern using bit-plane G0 from flash location 0. The second pattern is a 1-bit blue pattern using bit-plane G1 from flash location 0. The third pattern is a 1-bit red pattern using bit-plane G2 from flash location 0.

A pulse icon in between the patterns indicates that a trigger is needed between the patterns. Right-clicking on this icon allows the removal of the trigger, so two or more patterns can share the same trigger and are exposed in sequence for the total exposure time. Right-clicking on a pattern allows the option of inverting the pattern, removing the pattern, or inserting a black image by clearing the DMD after exposure time.

3.3.1.1 Pattern Sequence Example

To illustrate the Pattern Sequence mode, this section describes the steps to create a Gray Code sequence with Green LED. The DLPC350 firmware has several sets of images stored in the flash memory. Flash Image 8 corresponds to 24 1-bit gray code images that have been packed into a single 24-bit RGB bitmap. To load the pattern sequence, perform the following steps:

- Select Pattern Source: Flash
- Select Pattern Trigger Mode: Internal or External
- Set Timing of Internal Trigger: 100000 µs
- Set Pattern Exposure: 100000 µs
- Set Image Load Time: 200000 µs
- From the Individual Pattern Settings: Select Green and Internal Trigger
- Flash Image: Select 8
- For each 24 bit-plane of the packed 24-bit RGB image, select one bit-plane (a monochrome image) and add it to the pattern sequence by:

– Clicking on G0, then clicking the Add Pattern to Sequence button
– Clicking on G1, then clicking the Add Pattern to Sequence button

– Clicking on G2, then clicking the Add Pattern to Sequence button
– Clicking on G3, then clicking the Add Pattern to Sequence button
– Clicking on G4, then clicking the Add Pattern to Sequence button
– Clicking on G5, then clicking the Add Pattern to Sequence button
– Clicking on G6, then clicking the Add Pattern to Sequence button
– Clicking on G7, then clicking the Add Pattern to Sequence button
– Clicking on R0, then clicking the Add Pattern to Sequence button
– Clicking on R1, then clicking the Add Pattern to Sequence button
– Clicking on R2, then clicking the Add Pattern to Sequence button
– Clicking on R3, then clicking the Add Pattern to Sequence button
– Clicking on R4, then clicking the Add Pattern to Sequence button
– Clicking on R5, then clicking the Add Pattern to Sequence button
– Clicking on R6, then clicking the Add Pattern to Sequence button
– Clicking on R6, then clicking the Add Pattern to Sequence button
– Clicking on R7, then clicking the Add Pattern to Sequence button
– Clicking on B0, then clicking the Add Pattern to Sequence button
– Clicking on B1, then clicking the Add Pattern to Sequence button
– Clicking on B2, then clicking the Add Pattern to Sequence button
– Clicking on B3, then clicking the Add Pattern to Sequence button
– Clicking on B4, then clicking the Add Pattern to Sequence button
– Clicking on B5, then clicking the Add Pattern to Sequence button
– Clicking on B6, then clicking the Add Pattern to Sequence button
– Clicking on B7, then clicking the Add Pattern to Sequence button

• This forms 24 1-bit images that are displayed back-to-back at 100-ms exposure. Click on the Send button to download the pattern sequence to the DLP PRO4500.

3.3.2 Trigger Controls

The Trigger Controls subtab sets the polarity and adjusts the rising and falling edge delay of the trigger inputs and outputs, see Figure 3-6. The following trigger controls are available:

• TRIG_IN_1:

– Trigger 1 In Delay: Sets the rising edge delay of the DLPC350 TRIG_IN_1 signal in relation to the display of the pattern on the DMD. Each number adds 107.136 ns. The GUI allows for delay ranges between 0 µs and 28084.95 µs, but for more information on how to extend the delay range, see the DLPC350 Programmer's Guide DLPU010

• TRIG_OUT_1:

– Trigger 1 Out Rising Edge Delay: Sets the rising edge delay of the DLPC350 TRIG_OUT_1 signal in relation to the display of the pattern on the DMD. Each number adds 107.136 ns. Range is –20.05 µs (before pattern exposure) to +2.79 µs (after pattern exposure) delay.

– Trigger 1 Out Falling Edge Delay: Sets the falling edge delay of the DLPC350 TRIG_IN_1 signal in relation to the display of the pattern on the DMD. Each number adds 107.136 ns. Range is –20.05 µs (before pattern exposure) to +2.79 µs (after pattern

exposure) delay.

– Invert Trigger 1 out: Sets the polarity of the TRIG_OUT_1 signal. When unchecked, the polarity of TRIG_OUT_1 is active high. When checked, the polarity of TRIG_OUT_1 is active low.

• TRIG_OUT_2:

– Trigger 2 out Rising Edge Delay: Sets the rising edge delay of the DLPC350 TRIG_OUT_2 signal in relation to the display of the pattern on the DMD. Each number adds 107.136 ns. Range is –20.05µs (before pattern exposure) to +7.29 µs (after pattern exposure) delay.

– Invert Trigger 2 Out: Sets the polarity of the TRIG_OUT_2 signal. When unchecked, the polarity of TRIG_OUT_2 is active high. When checked, the polarity of TRIG_OUT_2 is active low.

– Patterns per Pulse see Figure 6: Indicates the number of patterns per TRIG_OUT_2 pulse.

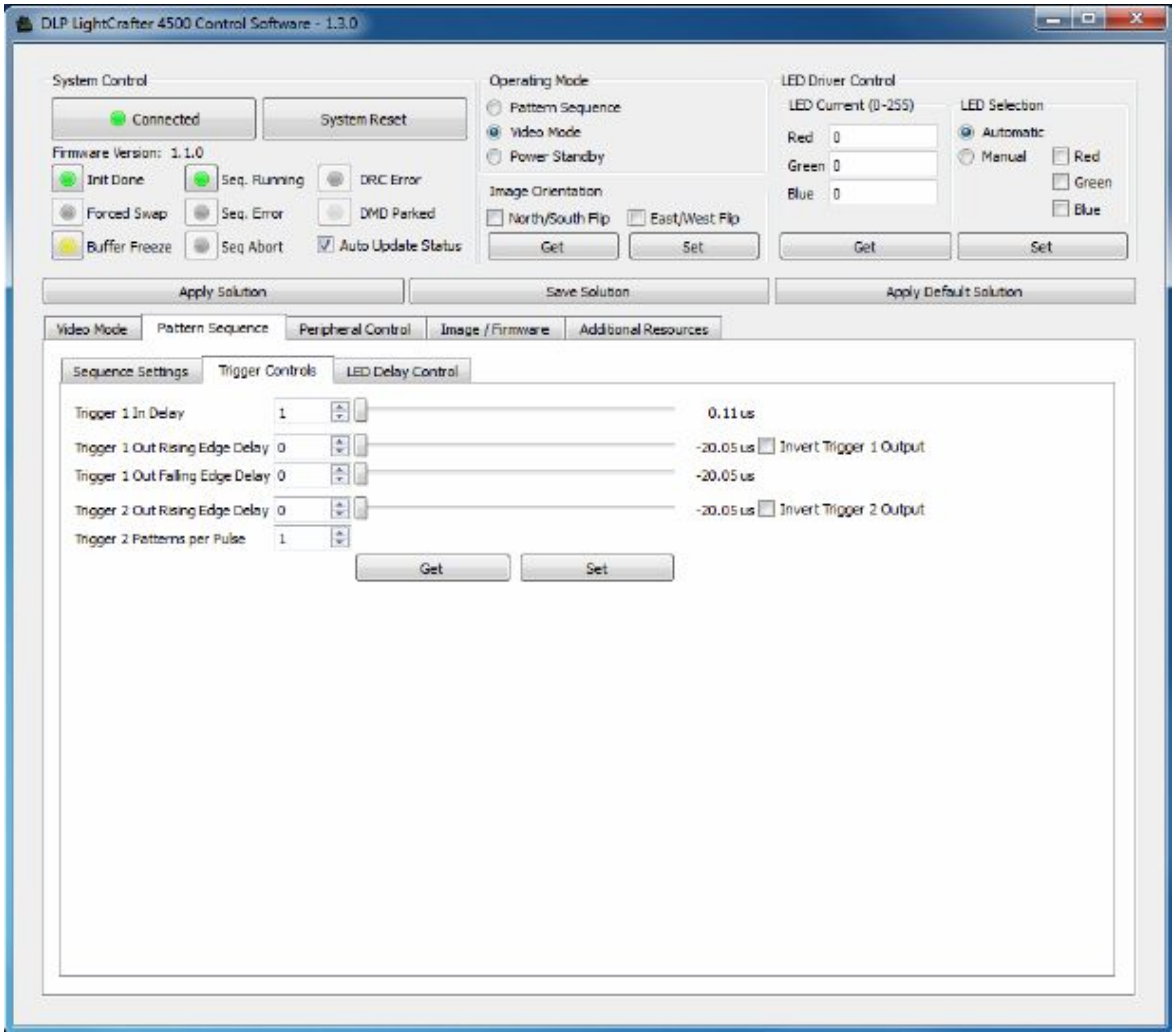

Figure 3-6. Trigger Control Subtab

The trigger output signals are:

• TRIG_OUT_1 frames the exposure time of the pattern.

• TRIG_OUT_2 indicates the start of the pattern sequence or internal buffer boundary of a 24-bit-plane.

examples of signals Figure 3-7 and Figure 3-8 show.

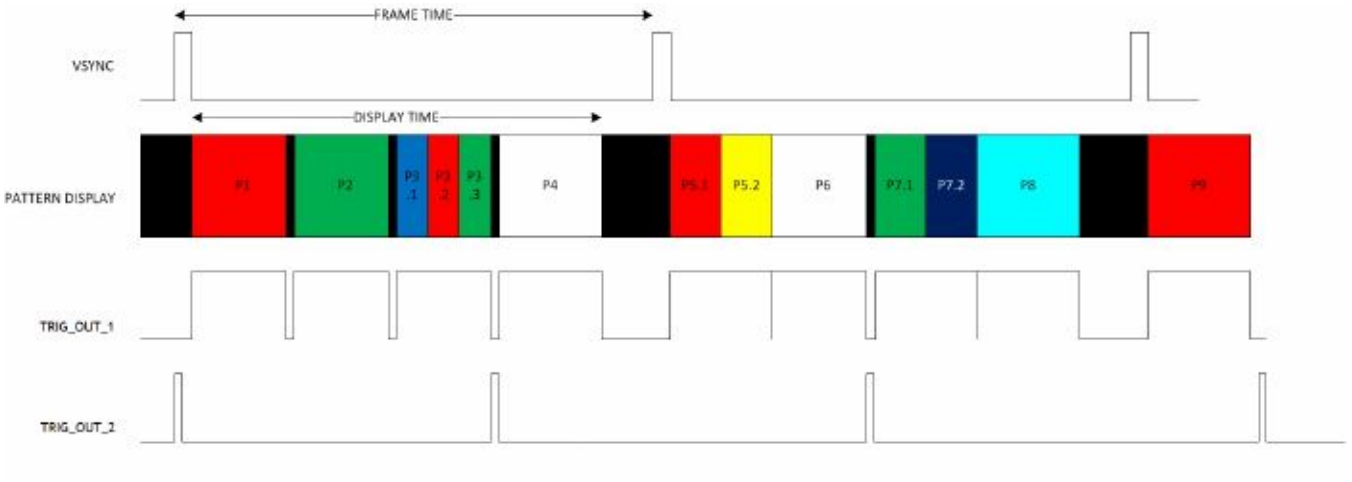

Figure 3-7. VSYNC Pattern Trigger Mode

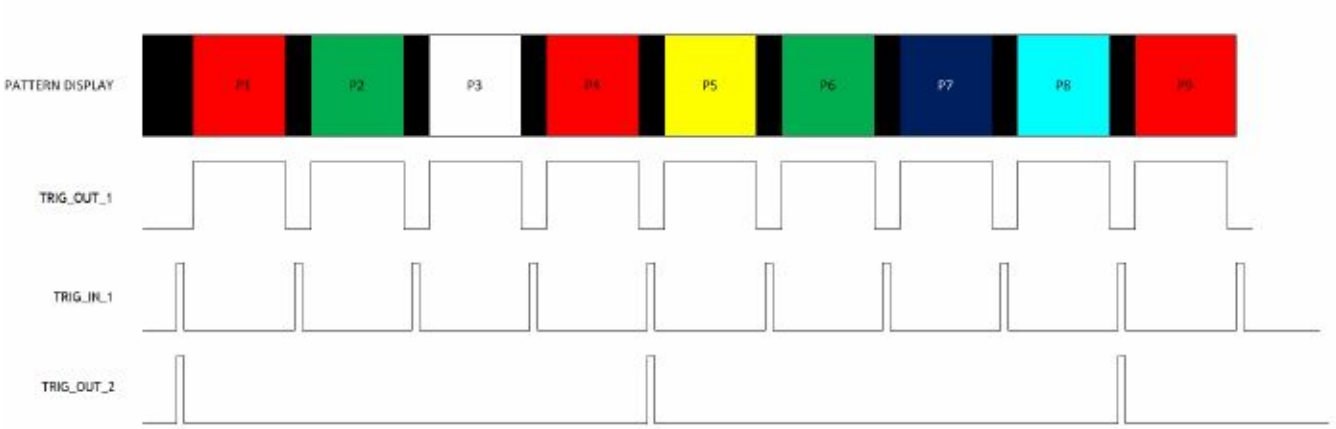

Figure 3-8. External Pattern Trigger Mode

3.3.3 LED Delay Control

In Pattern Sequence mode, the LED Delay Control subtab (see Figure 3-9) sets the rising and falling edge offsets of the LED enable signals in relation to the display of the pattern on the DMD. The rising and falling edge of the red, green, and blue LED enable signals can be independently changed between –20.05 µs (before pattern exposure) to +7.29 µs (after pattern exposure) delay.

When the PRO4500 is operating in Video Mode, set these delays to 0 (–20.05 µs).

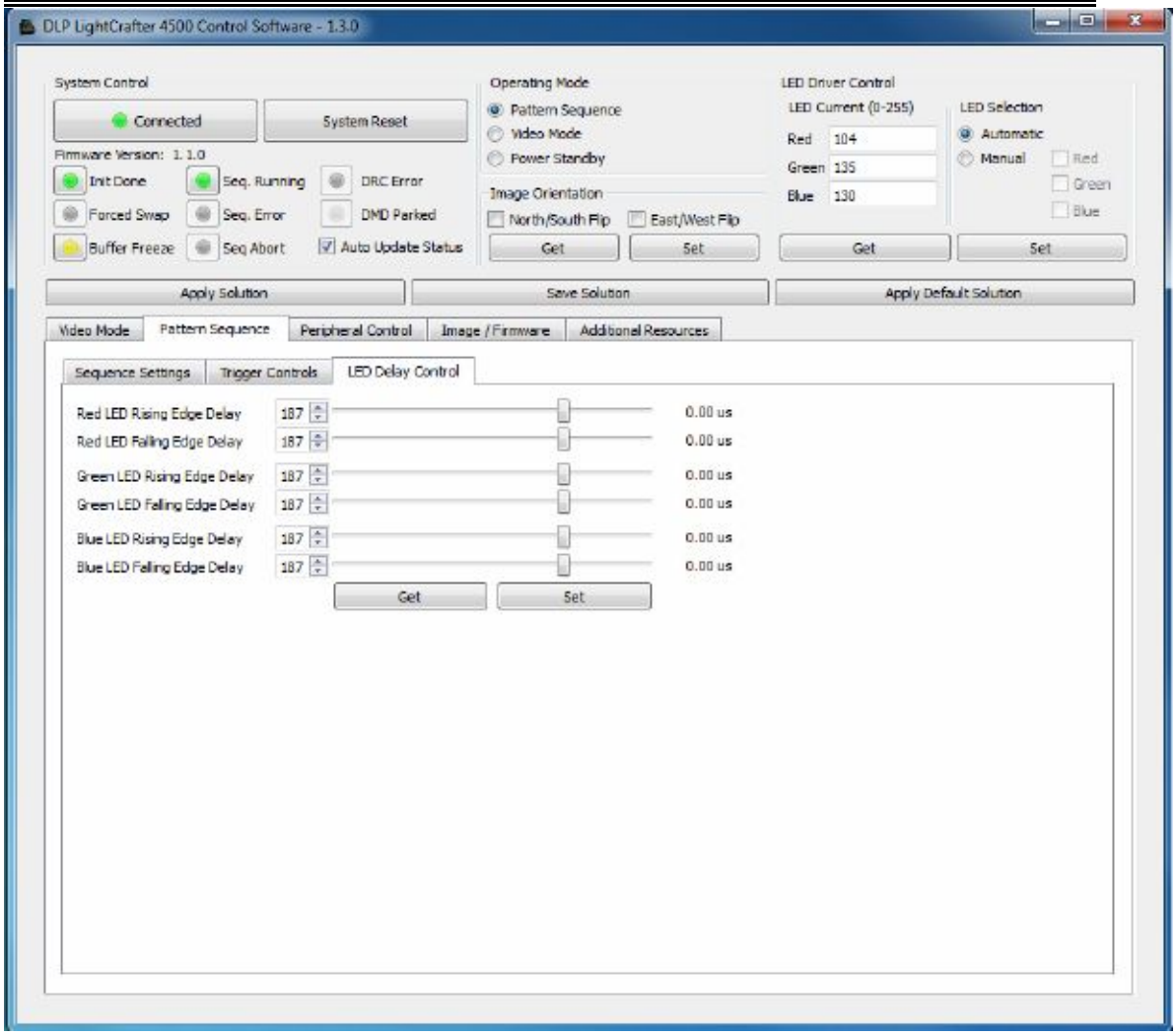

Figure 3-9. LED Delay Control Subtab

3.4 Firmware Upgrade

The PRO4500 GUI allows field updates of the DLPC350 firmware. To update the DLPC350 firmware, perform the following steps Figure 3-10

1. Select the Image / Firmware tab and the Firmware Upload subtab.
2. Click the Browse button to select the file to install.
3. Click the Upload button.
4. Wait for the upload process to complete. The flash memory is erased first, then rewritten with the new firmware image selected.

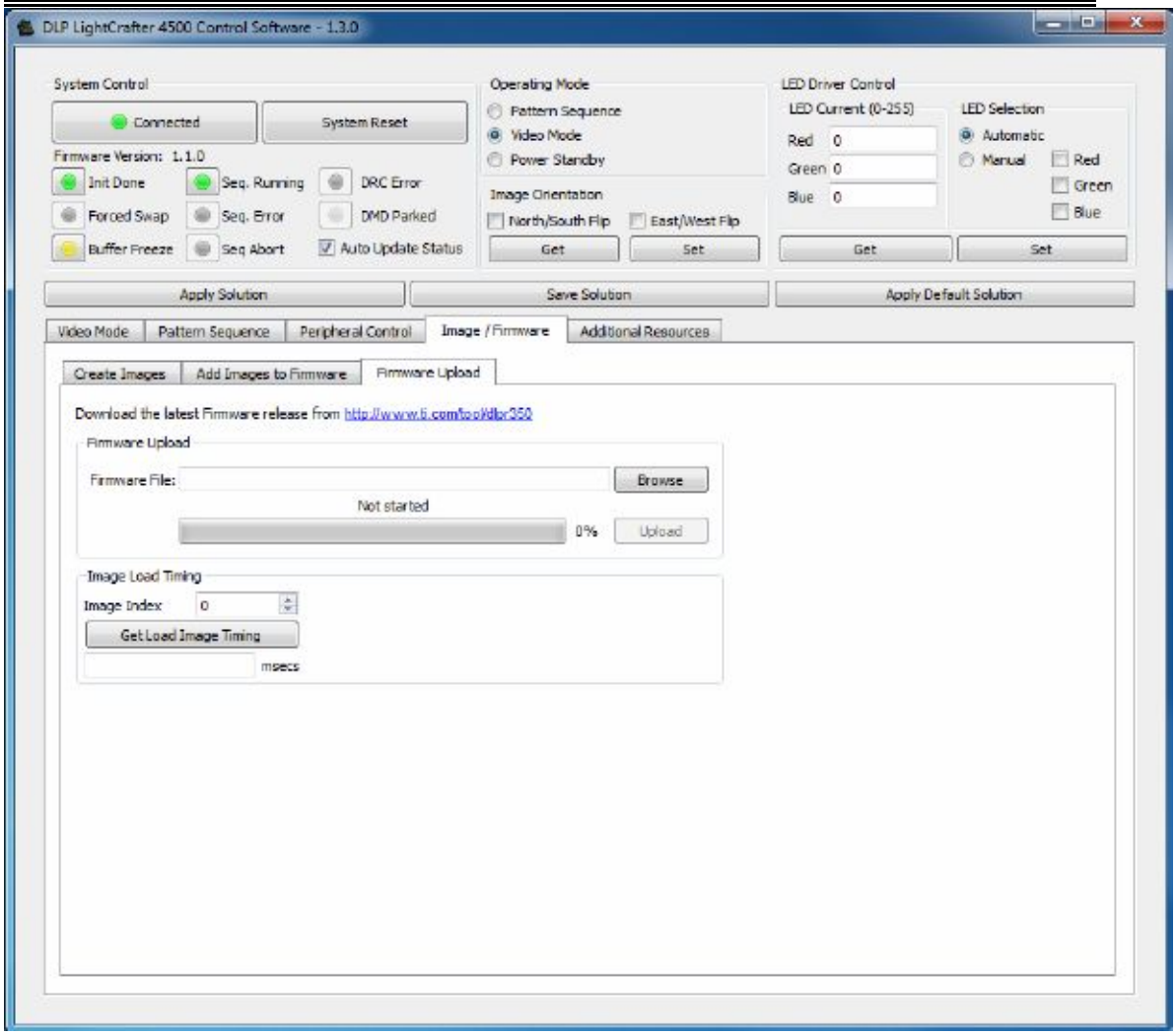

Figure 3-10. Firmware Upgrade Tab

3.5 Image Load Timing

The bottom section of the Firmware Upload section contains the Image Load Timing section. This section does an instant calculation on the time the DLPC350 takes to load a full 24-bit RGB bitmap from flash.

This measurement is instantaneous and is not the average nor worst-case timing. To get an instantaneous measurement, perform the following steps:

1. Select the desired image number from Image Index.
2. Click the Get Load Image Timing button.

The DLPC350 decompresses the 24-bit RGB bitmap stored at the Image Index location and loads it to the internal buffer. The time required for this process is displayed in milliseconds. This feature overwrites the images currently in the display buffer.

3.6 Storing Images in Flash Memory

PRO4500 allows images to be compressed and stored into the 32-MB flash memory. For most efficient storage and compression of images, stored images are packed into groups of 24-bit RGB bitmap images and decompressed on the fly while loaded from flash memory. To ease the packing of any bit width images, the PRO4500 GUI offers the Create Images subtab, see Figure 3-11. To create a 24-bit image from different multiple bit depth images, perform the following steps:

1. Select the Image / Firmware tab and the Create Images subtab.
2. Select a bitmap file with 912 columns by 1140 rows by clicking the...button next to Input bmp file
3. Select Output bitmap file by clicking the...button next to Output bmp file
4. For an input file, add the individual bit-planes by repeating the following process:
   (a) Set the bit depth and the bit field position with the Bit depth and the At bit position pulldown selectors, respectively.
   (b) Click the Add to Output File button. The current image is bit weighted and saved into the 24-bit image of the output file.

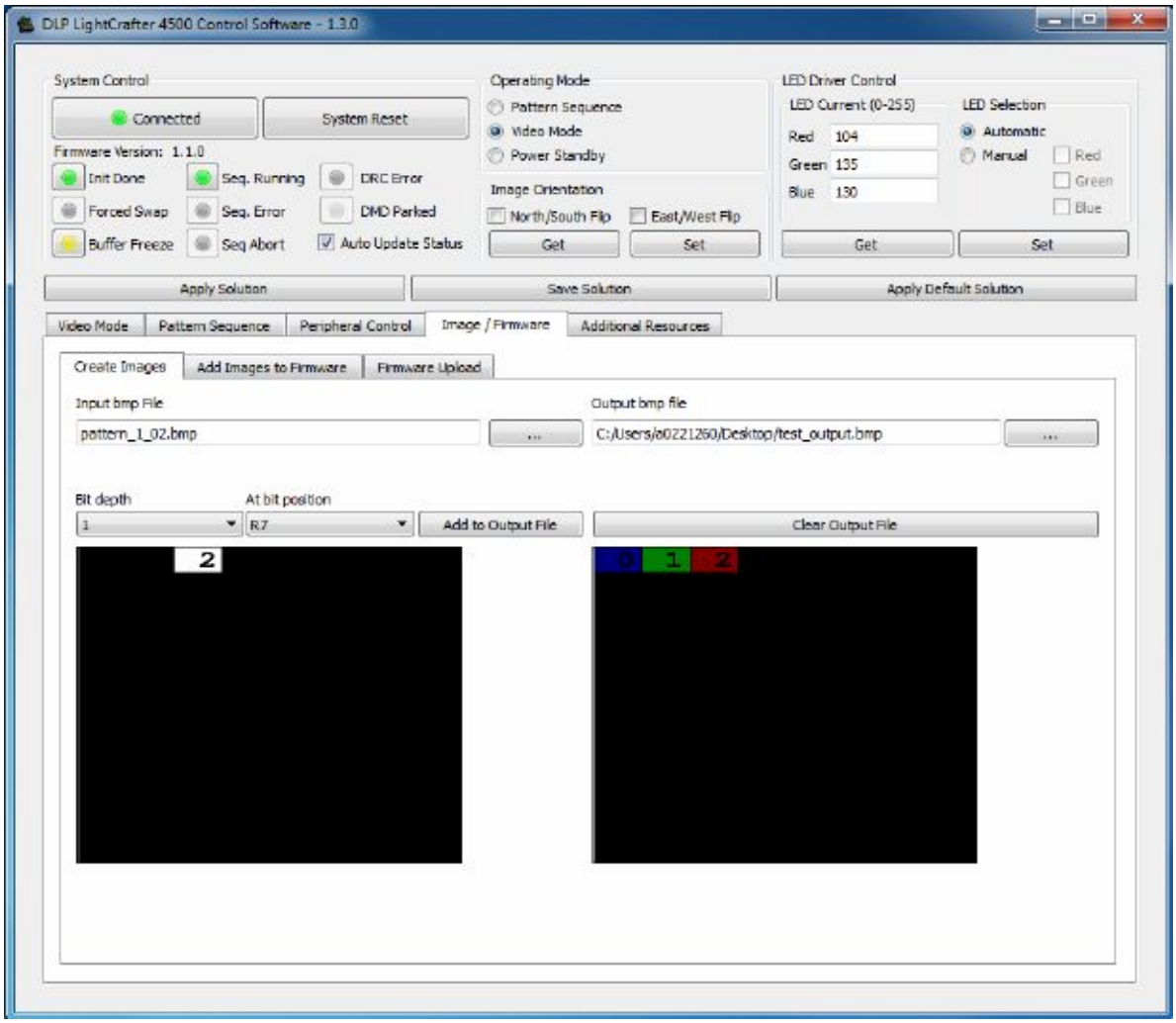

Figure 3-11. Create Images Tab

Underneath these selections, the left-hand window shows a preview of the Input file. The right-hand window shows a preview of the 24-bit output file that has taken all the input files and bit weighted the added images according to the bit-plane position requested. Images added at bit position B0 to B7 show blue, bit position G0 to G7 show green, and bit position R0 to R7 show red. For each color, bit position 0 is the least significant bit, while bit position 7 is the most significant bit.

To download the images into flash, a series of 24-bit images must be added to the firmware file using the Add Images to Firmware subtab with the following steps:
1. Select the Image / Firmware tab and the Add Images to Firmware subtab.
2. Select a firmware file by clicking the Browse button next to "Firmware File."
3. Add several 24-bit images by:
(a) Selecting the location of the image using the pulldown, and clicking the Add button. Browse the 24-bit image file created in the Create Images tab, and select it. The image is displayed next to these buttons.
4. If a new .ini file is desired, refer to Section 5.2. Otherwise, after adding all the images to the firmware, click the Save Updates button.
5. Download the firmware to the PRO4500 by following the steps for the Firmware Upgrade found in Section 3.4.

After clicking on "Build firmware", all the 24-bit images are compressed and packed together. The number of the image might differ from the one in the pulldown due to the packing of the 24-bit images.

3.7 GPIO Control

DLPC350 offers several configurable pins. The Peripheral Control tab of the GUI controls how these pins are configured. The following options are available:
• General Purpose Clock: Two DLPC350 pins can be individually configured as clocks.
• PWM Output Setup: Two DLPC350 pins, GPIO_00 (pin 18 in J6) and GPIO_02 (pin 22 in J6), can be individually set as PWM outputs.
• GPIO Configuration: Several DLPC350 pins can be individually configured as GPIO. Once configured as GPIO, the Pin Direction (Input or Output), if set to output the Pin State (High or Low) and output type (open drain output or drive high or low), can be configured. Some GPIO pins are already configured by the firmware for specific functions and these are listed with their current configuration.
• PWM Capture Setup: Two DLPC350 pins, GPIO_05 (pin 14 in J6) and GPIO_06 (pin 17 in J6), can be individually set as PWM inputs. These pins will sample at the frequency specified in PWM Sample Rate and report the duty cycle of the input signal.

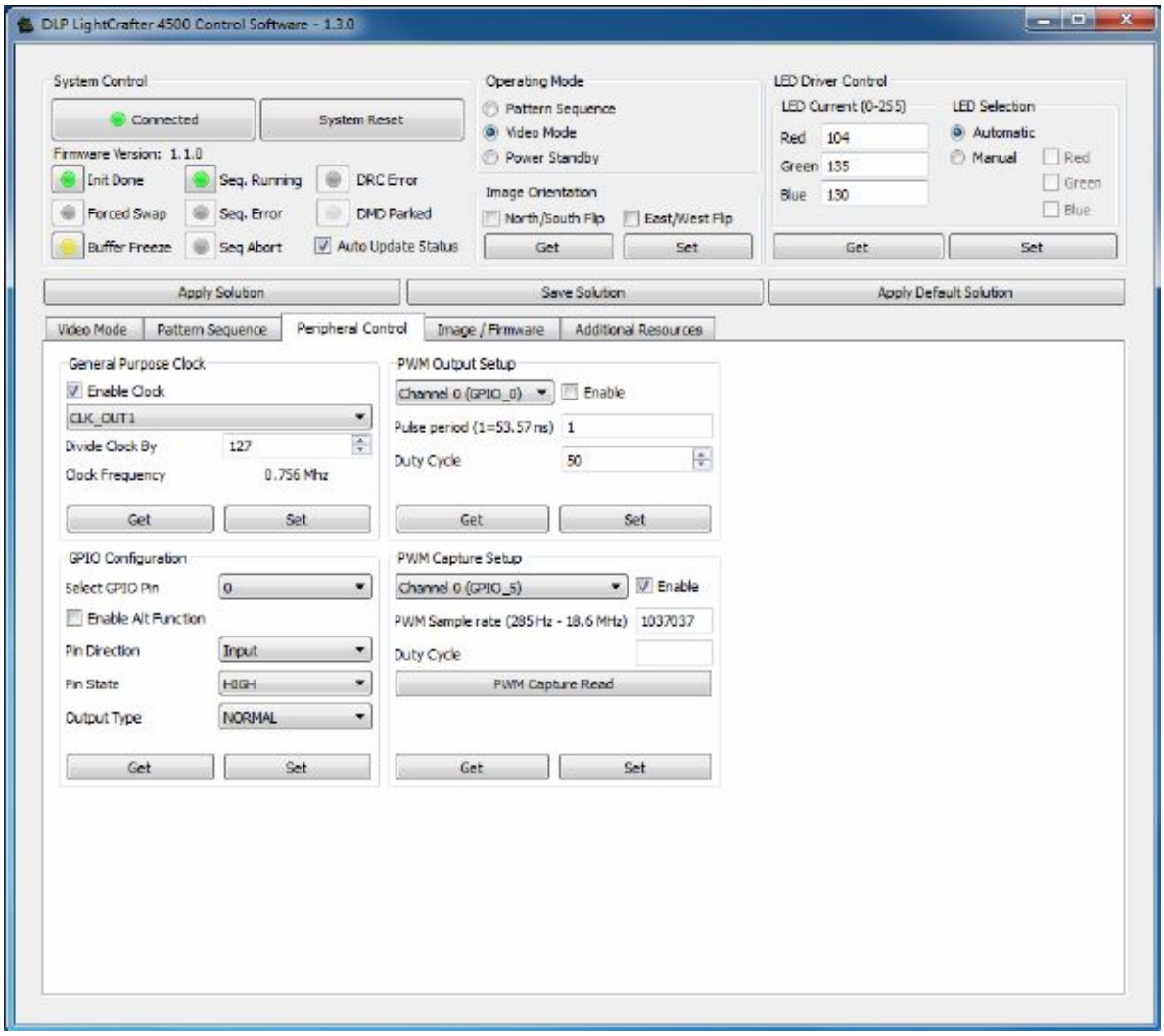

Figure 3-12. Peripheral Control Tab

Chapter 4 Pattern Sequences

This chapter describes the pattern sequences supported by the PRO4500 module.

4.1 Pattern Sequence Background

The DLPC350 takes as input 24-, 27-, or 30-bit RGB data at a frame rate of up to 120-Hz. This frame rate is composed of three colors (red, green, and blue) with each color equally divided in the 120-Hz frame rate. Thus, a 2.78-ms time slot is allocated to each color. Because each color has 8-, 9-, or 10-bit depth, each color time slot is further divided into bit-planes. A bit-plane is just a 1-bit representation of all the pixels in the image. For example, a 24-bit image is decomposed into its bit-planes in Figure 4-1.

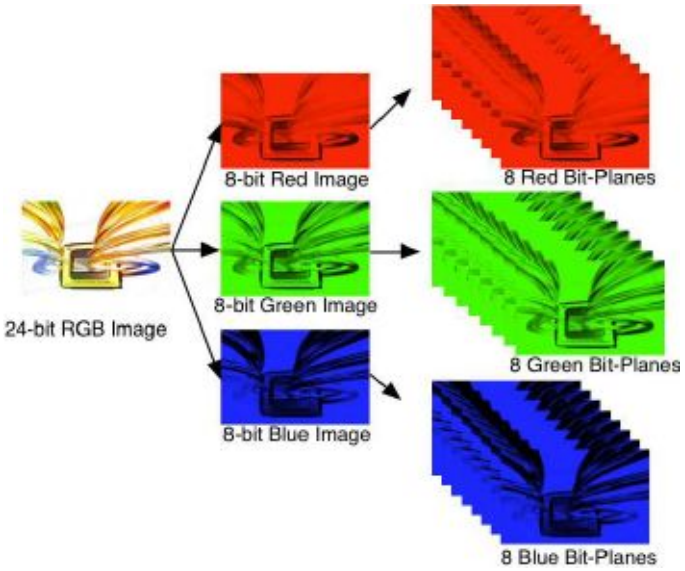

Figure 4-1. Relationship Between Bit-Planes and 24-bit RGB Images

The length of each bit-plane in the time slot is weighted by the corresponding power of 2 of its binary representation. This provides a binary pulse-width modulation of the image. For example, a 24-bit RGB input has three colors with 8-bit depth each. Each color time slot is divided into eight bit-planes, with the sum of all bit-planes in the time slot equal to 256. Figure 4-2 shows this partition of bits in a frame.

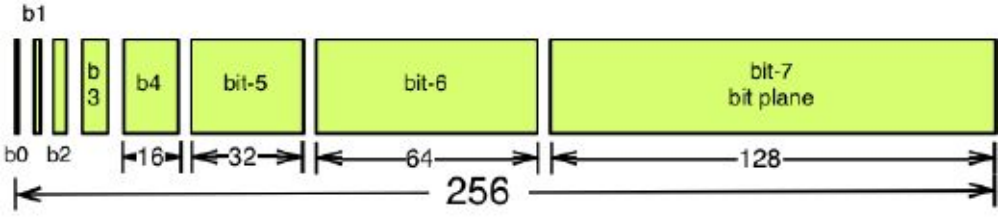

Figure 4-2. Bit Partition

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane.

With binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on. For a 24-bit RGB frame image loaded to the DLPC350, the DLPC350 creates 24 bit-planes, stores them in its internal display buffer, and sends the bit-planes to the DLP4500 DMD, one bit-plane at a time. Depending on the bit weight of the bit-plane, the DLPC350 controls the time this bit-plane is exposed to light, controlling the intensity of the bit-plane. To improve image quality in video frames, the bit-planes, time slots, and color frames are intertwined and interleaved with spatial-temporal algorithms by the DLPC350.

For other applications where this image enhancement is not desired, the video processing algorithms can be bypassed and replaced with a specific set of bit-planes. The bit depth of the pattern is then allocated into the corresponding time slots. Furthermore, an output trigger signal is also synchronized with these time slots to indicate when the image is displayed. For structured light applications, this mechanism provides the capability to display a set of patterns and signals for the camera to capture these patterns overlaid on an object.

As shown in Figure 4-3, the DLPC350 stores two 24-bit frames in its internal memory buffer. This 48 bit-plane display buffer allows the DLPC350 to send one 24-bit buffer to the DMD array while the second buffer is filled from flash or streamed in through the 24-bit parallel RGB or FPD-link interface. In streaming mode, the DMD array displays the previous 24-bit frame while the current frame fills the second 24-bit frame of the display buffer. Once a 24-bit frame is displayed, the buffer rotates providing the next 24-bit frame to the DMD. Thus, the displayed image is a 24-bit frame behind the data streamed through the 24- bit RGB parallel or FPD-link interface.

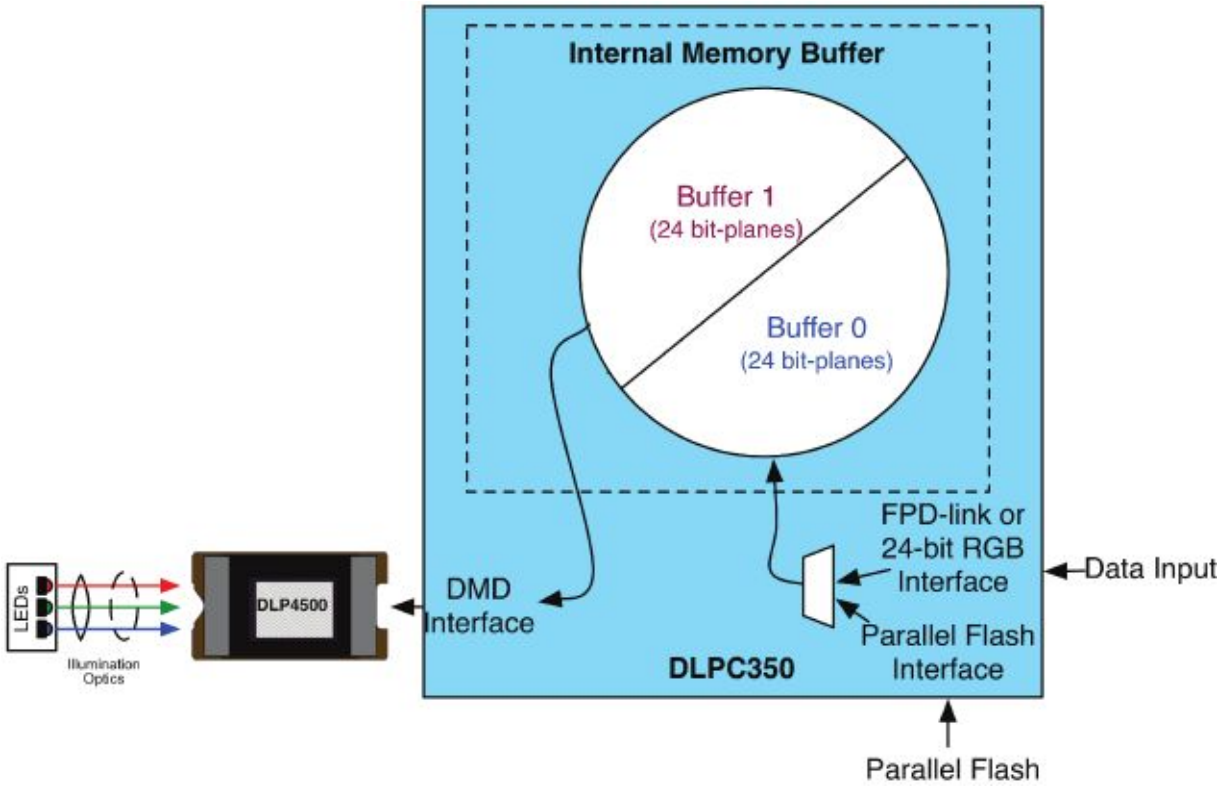

Figure 4-3. DLPC350 Internal Memory Buffer

When the PRO4500 is set to Video Mode, the displayed image is a frame delayed in relation to the data streamed through the RGB parallel interface or FPD-link, as shown in Figure 4-4.

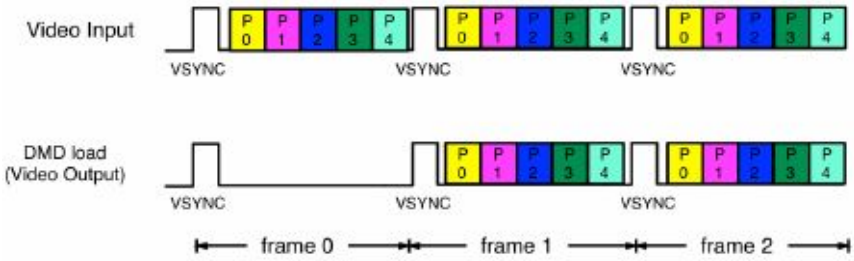

Figure 4-4. Frame Delay Between Parallel Interface Input and Projection Output

When the PRO4500 is set to Pattern Sequence mode with pattern source from flash, the pattern sequence must be loaded from flash memory. The DLPC350 takes at-worst-case 200 ms to load one buffer (24 bit-planes). The actual time to load the buffer depends on the complexity of the image. The actual time is provided in the Image / Firmware tab under Image Load Time. If the pattern sequence is less than 24 bit fields, the patterns are displayed from a preloaded buffer. Once the patterns are loaded, the pattern sequence repeats from the internal display memory with no buffer load penalty. If the pattern sequence is greater than 24 bit-fields, the 24 bit-field pattern sequence display time must be longer than the full buffer load time. This provides enough time to load the next buffer

while the current buffer is displayed. See Figure 4-5 for a diagram of Image Load Time, Pattern Exposure Trigger period, and Internal Trigger period.

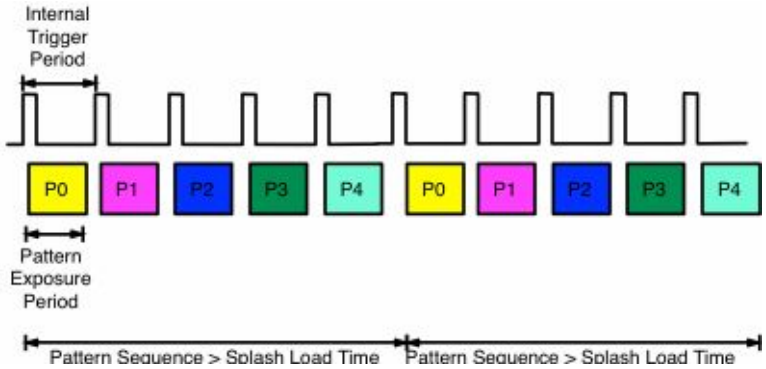

Figure 4-5. Image Load Time and Pattern Sequence Timing

In pattern sequence mode, the 48 bit-planes can be preloaded from flash memory and then sequenced with a combination of patterns with different bit depths. To synchronize a camera to the displayed patterns, the DLPC350 supports two trigger inputs and two trigger outputs. TRIG_IN_1 pulse indicates to the DLPC350 to advance to the next pattern, while TRIG_IN_2 starts and stops the pattern sequence.

TRIG_OUT_1 frames the exposure time of the pattern, while TRIG_OUT_2 indicates the start of the pattern sequence or internal buffer boundary of 24 bit-planes. For example, in Figure 3-7, the VSYNC starts the pattern sequence display. The pattern sequence consists of a series of three consecutive patterns. The first pattern sequence consists of P1, P2, and P3. P3 is an RGB pattern, it is shown with its time-sequential representation of P3.1, P3.2, and P3.3. The second pattern sequence consists of three patterns: P4, P5, and P6. The third sequence consists of P7, P8, and P9. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each of the three pattern sequences. In Figure 3-8, a pattern sequence of a group of four patterns are displayed. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each four-pattern sequence. TRIG_IN_1 pulses advance the pattern.

Table 4-1 lists the allowed pattern combinations in relation to the bit depth of the external pattern.

Table 4-1. Allowable Pattern Combinations

Bit Depth	External RGB Input Pattern Rate (Hz)	Preloaded Pattern Rate (Hz)	Minimum Pattern Exposure Period (µs)	Maximum Number of Patterns using Two Buffers(PreLoaded)
1 bit	2880	4225	235	48
2 bits	1428	1428	700	24
3 bits	636	636	1570	16
4 bits	588	588	1700	12
5 bits	480	500	2000	8
6 bits	400	400	2500	8
7 bits	222	222	4500	6
8 bits	120	120	8333	6

Chapter 5 Saving Solutions

On GUI software version 1.2 or later, any of the parameters set on the GUI can be stored as a solution. This solution can later be recalled with a single button or set to run as default on powerup. Temporary solutions are essentially .ini files that contain all the current parameter settings on the GUI. The .ini file is stored on the PC. To create a new default solution, you must build the .ini file into a new firmware image. This chapter describes the processes for creating, loading, and storing solutions.

5.1 Applying Solutions

This feature refers to the temporary solutions saved as .ini files on the PC. Three buttons in the static panel of the GUI control the application and creation of these solutions:Apply Solution,Save Solution, and Apply Default Solution.

- **Apply Solution**: Click this button to browse for .ini solutions that are already saved. Upon selecting an .ini file, the corresponding parameters update in the GUI. Parameters the user cannot change in the GUI (version number and splash time-out) do not take effect.
- **Apply Default Solution**: This button restores the settings to match those of the original DLPC350 firmware. Clicking this button is effectively the same as saving a solution and only selecting the values in the first column of radio buttons.
- **Save Solution**: Click this button to make a new window with a list of several parameters (described in Section 5.3.1) appear. One column of radio buttons contains the values set in the original DLPC350 firmware. The second column of radio buttons contains the values currently set in the GUI. The user can select either the original or current values to store in the .ini file

5.2 Changing Default Solutions

This feature refers to the process of taking an .ini file and building it into a new firmware image. The following procedure should be followed:

1. Select the Image / Firmware tab and the Add Images to Firmware subtab.
2. Choose a base firmware file. The Select .ini File button becomes active and lets the user browse for an .ini file.
3. Once the .ini file is selected, click the Save Updates button to save a new firmware image file.
4. Upload this new .bin or .img file to the PRO4500. The PRO4500 boots with the settings specified in the .ini file, and returns to these settings if reset.

CAUTION

Before saving an .ini to firmware, TI recommends first applying the solution. Wrong values or incorrect syntax can potentially damage the DLP PRO4500.

5.3 Modifying .ini Files

There are two ways to modify the .ini files. The first method is to use the Save Solution button on the GUI. The second method is to open the .ini file in a text file editor and edit it manually.

5.3.1 Available Parameters

Table 5-1 lists all available parameters. For more details read the Programmer's Guide (DLPU010).

Table 5-1. List of Available Parameters when Saving Solutions

Parameter Name	Programmer's Guide Command	Extra Notes
APPCONFIG.VERSION.SUBMINOR	Retrieve Firmware Version	Corresponds to: Application software patch number. Range: 0x0000 to 0xFFFF
DEFAULT.AUTOSTART	N/A	0x0 = Boot normally 0x1 = Boot in standby
DEFAULT.DISPMODE	Display Mode Selection	0x0 = Video mode 0x1 = Pattern display mode (will start pattern sequence after initialization and splash time-out)
DEFAULT.SHORT_FLIP	Short-Axis Image Flip	0x0 = Disable 0x1 = Enable
DEFAULT.LONG_FLIP	Long-Axis Image Flip	0x0 = Disable 0x1 = Enable
DEFAULT.TRIG_OUT_1.POL	Trigger Out1 Control	0x0 = Active high 0x1 = Active low
DEFAULT.TRIG_OUT_1.RDELAY	Trigger Out1 Control	Each can range from 0x00 and 0xD5
DEFAULT.TRIG OUT_1.FDELAY		
DEFAULT.TRIG_OUT_2.POL	Trigger Out2 Control	0x0 = Active high 0x1 = Active low
DEFAULT.TRIG_OUT_2.WIDTH	Trigger Out2 Control	Range: 0x00 to 0xFF
DEFAULT.TRIG_IN_1.DELAY	Trigger In1 Control	Range: 0x00 to 0xFF
DEFAULT.TRIG_IN_2.POL	Trigger In2 Control	For Trigger mode 2 only
DEFAULT.RED_STROBE.RDELAY	Red LED Enable Control	Range: 0x00 to 0xFF
DEFAULT.RED_STROBE.FDELAY		
DEFAULT.GRN_STROBE.RDELAY	Green LED Enable Control	Range: 0x00 to 0xFF
DEFAULT.GRN_STROBE.FDELAY		
DEFAULT.BLU_STROBE.RDELAY	Blue LED Enable Control	Range: 0x00 to 0xFF

DEFAULT.BLU_STROBE.FDELAY		
DEFAULT.INVERTDATA	Pattern Display Invert Data	0x0 = Typical operation 0x1 = Inverted operation
DEFAULT.LEDCURRENT_RED	LED Driver Current Control	Range: 0x00 to 0xFF. On this reference design, 0x0 is the maximum PWM, and 0xFF is the minimum. If multiple LEDs are enabled simultaneously (pattern mode or manual operation), then be mindful of maximum current values for design.
DEFAULT.LEDCURRENT_GRN		
DEFAULT.LEDCURRENT_BLU		
DEFAULT.PATTERNCONFIG.PAT_EXPOSURE	Pattern Display Exposure and Frame Period	PAT_EXPOSURE must be less than PAT_PERIOD by at least 230 µs, or it must be equal to PAT_PERIOD.
DEFAULT.PATTERNCONFIG.PAT_PERIOD		
DEFAULT.PATTERNCONFIG.PAT_MODE	Pattern Display Data Input Source	0x0 = Streaming patterns through video ports 0x3 = Flash memory
DEFAULT.PATTERNCONFIG.TRIG_MODE	Pattern Trigger Mode Selection	0x0 = Vsync trigger 0x1 = Internal or external trigger 0x2 = Alternating trigger (not currently in GUI)
DEFAULT.PATTERNCONFIG.PAT_REPEAT	Pattern Display LUT Control	0x0 = Play once 0x1 = Repeat the pattern sequence
DEFAULT.PATTERNCONFIG.NUM_SPLASH	Pattern Display LUT Control	Must be less than 63 (where 0x0 = 1, and 0x3F = 64). Must equal number of items in DEFAULT.SPLASHLUT
DEFAULT.SPLASHLUT	Pattern Display LUT Data–Image Index	Flash image indexes in the order they appear in the pattern sequence. (Example: DEFAULT.SPLASHLUT 0x1 0x2 0x1 0x3 0x0 0x2)
DEFAULT.PATTERNCONFIG.NUM_LUT_ENTRIES	Pattern Display LUT Control	Must be less than 128 (where 0x0 = 1, and 0x7F = 128). Must equal number of items in DEFAULT.SEQPATLUT.
DEFAULT.PATTERNCONFIG.NUM_PATTERNS	Pattern Display LUT Control	If PATTERNCONFIG.PAT_REPEAT = 0x0, then should equal number of items in DEFAULT.SEQPATLUT. If PAT_REPEAT = 0x1, then should equal number of patterns between desired Trigger Out2 pulses.
DEFAULT.SEQPATLUT	Pattern Display LUT Data – Pattern Definition	Example for two patterns: DEFAULT.SEQPATLUT 0x00042100 0x00002104;
DEFAULT.PORTCONFIG.PORT	Input Source Selection	0x0 = Parallel interface 0x1 = Internal test pattern 0x2 = Flash 0x3 = FPD-Link
DEFAULT.PORTCONFIG.BPP	Input Source Selection	0x0 = 30-bit 0x1 = 24-bit 0x2 = 20-bit 0x3 = 16-bit 0x4 = 8-bit
DEFAULT.PORTCONFIG.PIX_FMT	Input Pixel Data Format	0x0 = RGB 0x1 = YCrCb 444 0x2 = YCrCb 422
DEFAULT.PORTCONFIG.PORT_CLK	Port Clock Select	0x0 = A (needed for this reference design) 0x1 = B 0x2 = C
DEFAULT.PORTCONFIG.ABC_MUX	Input Data Channel Swap Command	0x1 – ABC = CAB 0x2 – ABC = BCA 0x3 – ABC = ACB 0x4 – ABC = BAC 0x5 – ABC = CBA
DEFAULT.PORTCONFIG.PIX_MODE	FPD-Link Mode and Field Select	0x0 = Mode 1 0x1 = Mode 2 0x2 = Mode 3 0x3 = Mode 4
DEFAULT.PORTCONFIG.SWAP_POL	FPD-Link Mode and Field Select	0x0 = Typical 0x1 = Inverted

DEFAULT.PORTCONFIG.FLD_SEL	FPD-Link Mode and Field Select	0x0 = CONT1 0x1 = CONT2 0x2 = Force 0
PERIPHERALS.I2CADDRESS[0]	I2C Interface in Interface Protocol Section	
PERIPHERALS.I2CADDRESS[1]		
DATAPATH.SPLASHSTARTUPTIMEOUT	N/A	Time in milliseconds before default image times out. Range: 0x0000 to 0xFFFF
DATAPATH.SPLASHSTARTUPENABLE	N/A	0x0 = Do not show a default image when board initializes (powerup or reset) 0x1 = Show a default image when board initializes (powerup or reset)

5.3.2 Save Solution Button

When this button is clicked in the GUI, a new window with a subset of parameters from Table 5-1 appear. One column of radio buttons contains the original values of the DLPC350 firmware. The second column of radio buttons contains the values currently set in the GUI. Select which value or values you want in your .ini file. This method is the preferred way of previewing syntax errors or invalid entries.

5.3.3 Manual Editing

The .ini files can be edited as text files. This method does not check syntax or validate commands. TI recommends this method only for editing those commands not available through the GUI (APPCONFIG.VERSION.SUBMINOR, DEFAULT.AUTOSTART, PERIPHERALS.I2CADDRESS, DATAPATH.SPLASHSTARTUPTIMEOUT, and DATAPATH.SPLASHSTARTUPENABLE). This method can be used with the LUT Helper Tool provided in the software bundle for DEFAULT.SPLASHLUT and DEFAULT.SEQPATLUT. For more information about the tool, Section 5.3.4.

5.3.4 LUT Entry Helper Tool

The LUT Entry Helper Tool has four tabs. The first two tabs can be used to calculate the values for DEFAULT.SEQPATLUT and DEFAULT.SPLASHLUT. The second two tabs are for reference.

5.3.4.1 Pattern LUT Entries

This tab is used to calculate the values for DEFAULT.SEQPATLUT. The table with 128 possible entries can be modified with the desired parameters for each pattern in the pattern sequence. It is possible to customize various parameters for each pattern. Valid entries for each category below are found in the Data tab.

- BIT-DEPTH: Select between 1 and 8.
- PATTERN: Select the desired pattern number. Each bit-depth of n corresponds to a pattern number equal to 24 / n. See the Pattern Bit-Planes tab to understand the mapping of bit-planes to pattern number.

• LED: Select which LEDs are on.
• TRIG IN: Select the type of trigger input that will trigger the current pattern. If streaming through the video port, the VSYNC acts as the External Positive trigger, and any subsequent patterns in the frame (between VSYNC pulses) have no trigger. These patterns are labeled with "Continue" in the Pattern Sequence window.
• PAT INVERT: Select whether or not to invert the pattern.
• INSERT BLK: Select whether to clear the DMD after each pattern or not. TI recommends clearing the DMD at least after the last pattern in the LUT.
• BUFF SWAP: This parameter indicates whether or not to move to the next flash image in the SPLASHLUT. Each time this is a yes, the SPLASHLUT index increments. The index returns to 0 if there are no more indexes.
• TRIG OUT: Either a new Trigger Out1 is generated (NEW) or the pattern shares exposure time with the previous pattern (PREV) and no output trigger is generated.

As the user changes the values in the LUT, the values in the LUT DATA column change. After entering the parameters for as many patterns as needed, scroll to the bottom of the sheet. Enter the total number of patterns next to N = (in cell C138). Then, row 139 generates the necessary values the user must copy into the .ini file.

Lastly, there is a Debug Helper tool at the bottom of this sheet. Enter a hex code where it says LUT DATA to find out what the corresponding parameters are.

5.3.4.2 Image LUT Entries

This tab is used to calculate the values for DEFAULT.SPLASHLUT. This tab converts the desired image indexes into hexadecimal values. Row 6 contains the calculated string of values for your .ini file. If the user repeats indexes, enter them separately. See this example in Table 5-2; the order is 0, 13, 12, 1, 13, 12, 0, 13, 12, 1, 13, 12, and so on.

Table 5-2. Image LUT Entries Example

SL No.	1	2	3	4	5	6
Image Index in Decimal	0	13	12	1	13	12
DEFAULT.SPLASHLUT	0x0	0xD	0xC	0x1	0xD	0xC

Chapter 6 ELC4460 Interface

This chapter describes the interface between the PRO4500 and the ELC4460.

6.1 ELC4460

ELC4460 is a low-cost platform based on the TI OMAP4 application processor. The PRO4500combined with a ELC4460 provides users with an embedded platform that eliminates the need for a dedicated laptop or PC. The ELC4460 includes an OMAP4 1.2-GHz, dual-coreprocessor, 1GB of onboard RAM, 8GB EMMC flash,TF card slot, and a suite of connectivity options, including:

- Ethernet,Bluetooth ®
- USB 2.0
- HDMI output.

The combination of ELC4460 with PRO4500 allows for the creation of self-contained, high-precision mobile tools to meet a growing number of applications, such as inline machine vision systems, portable, high-accuracy 3D scanners, and field spectrometers.
ELC4460can interface with the PRO4500 directly.

Figure 6-1. PRO4500 With ELC4460

6.1.1 PRO4500 to ELC4460 Interface

As shown in Figure 6-2, the PRO4500 supplies 5-V power to the ELC4460. The ELC4460 provides 1.8 V to the PRO4500 to level-shift all the signals interfacing the two boards together. The following OMAP4 GPIOs control the routing of OMAP4 peripherals to the corresponding DLPC350 peripherals:

- To power down the output of TFP401 and enable the level shifters in the 24-bit RGB interface, the OMAP4 processor must drive GPIO_140 (SYS_MSTR_MUX_SEL) high.
- To connect the OMAP4 USB3 bus to the DLC350, OMAP4 must drive GPIO_39 (SYS_USB_SEL) high.
- To connect the OMAP4 I2C2 bus to the DLPC350 I2C1 bus, OMAP4 must drive GPIO_51 (SYS_I2C_OE) high.
- To disconnect UART output of DLPC350 from J20 and route it to OMAP4 UART4, OMAP4 must drive GPIO_33 high.
- To connect the triggers from DLPC350 to OMAP4 GPIOs, OMAP4 must drive GPIO_61 (SYS_TRIGGER_SEL) high.

Table 6-1, Table 6-2, Table 6-3, and Table 6-4 list the signals interfacing the OMAP4 processor in the ELC4460 with the DLPC350 in the PRO4500.

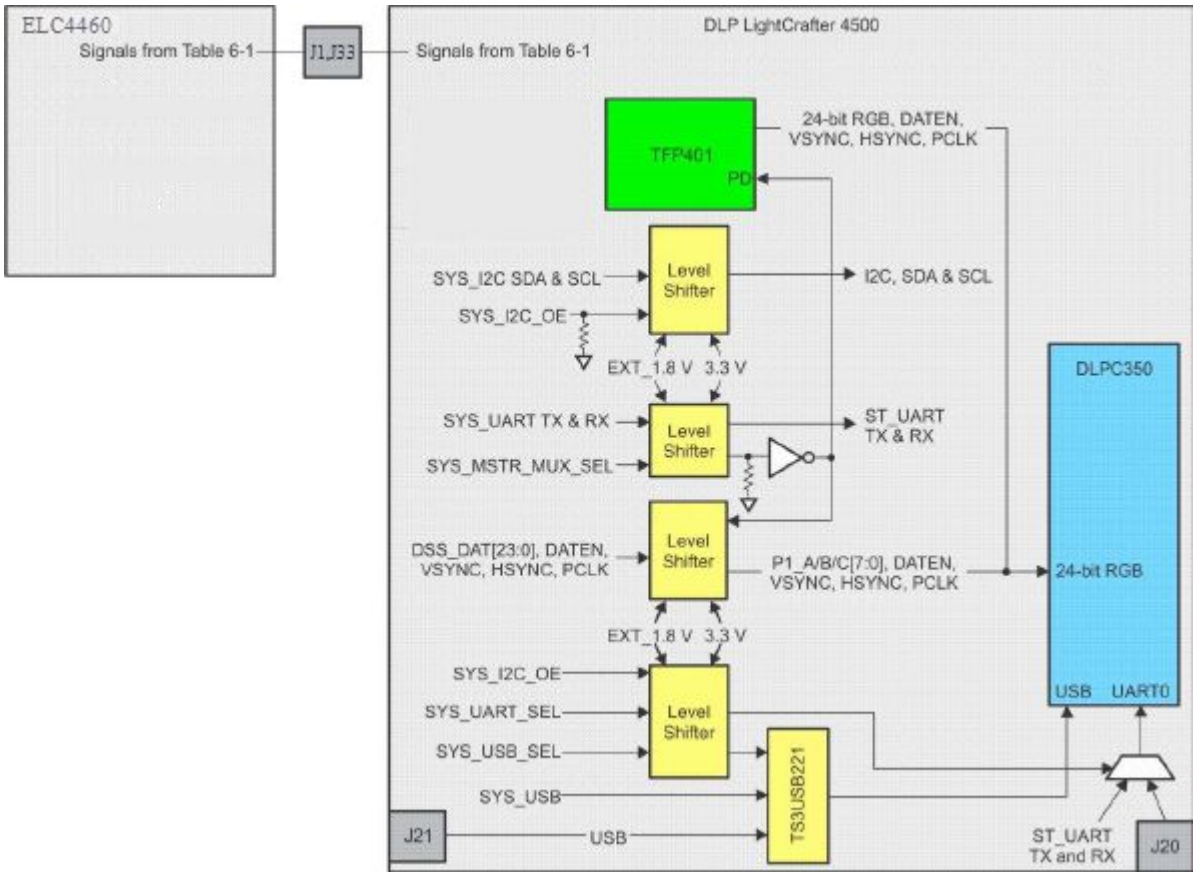

Figure 6-2. Block Diagram of the ELC4460 Interface

Table 6-1. J32ELC4460 to PRO4500 Interface

Pin	ELC4460 J1			PRO4500J32
	I/O	Signal	Description	
1	DCIN_JACK	PWR	5 V supplied from PRO4500	PP5P0V
2	DCIN_JACK	PWR	5 V supplied from PRO4500	PP5P0V
3	h_DSS_DAT1	O	OMAP4 LCD pixel data bit 1	SYS_DATA01
4	h_DSS_DAT0	O	OMAP4 LCD pixel data bit 0	SYS_DATA00
5	h_DSS_DAT3	O	OMAP4 LCD pixel data bit 3	SYS_DATA03
6	h_DSS_DAT2	O	OMAP4 LCD pixel data bit 2	SYS_DATA02
7	h_DSS_DAT5	O	OMAP4 LCD pixel data bit 5	SYS_DATA05
8	h_DSS_DAT4	O	OMAP4 LCD pixel data bit 4	SYS_DATA04
9	h_DSS_DAT12	O	OMAP4 LCD pixel data bit 12	SYS_DATA012
10	h_DSS_DAT10	O	OMAP4 LCD pixel data bit 10	SYS_DATA010
11	h_DSS_DAT23	O	OMAP4 LCD pixel data bit 23	SYS_DATA023
12	h_DSS_DAT14	O	OMAP4 LCD pixel data bit 14	SYS_DATA014
13	h_DSS_DAT19	O	OMAP4 LCD pixel data bit 19	SYS_DATA019
14	h_DSS_DAT22	O	OMAP4 LCD pixel data bit 22	SYS_DATA22
15	h_I2C2_SDA	I/O	OMAP4 I2C2 Serial Data	SYS_I2C1_SDA
16	h_DSS_DAT11	O	OMAP4 LCD pixel data bit 11	SYS_DATA11
17	h_DSS_VSYNC	O	OMAP4 LCD Vertical Sync Signal	SYS_VSYNC
18	NC		No Connect	NC
19	DGND	GND	Ground bus	GND
20	DGND	GND	Ground bus	GND
21	VDD_VAUX2	PWR	ELC4460 Power rail(adjustable from 1.2 V to 2.8 V)	VDD_AUX2
22	VIO_1V8	PWR	ELC4460 1.8 V system I/O voltage	EXT_1V8
23	h_DSS_DAT20	O	OMAP4 LCD pixel data bit 20	SYS_DATA20
24	h_DSS_DAT21	O	OMAP4 LCD pixel data bit 21	SYS_DATA21
25	h_DSS_DAT17	O	OMAP4 LCD pixel data bit 17	SYS_DATA17
26	h_DSS_DAT18	O	OMAP4 LCD pixel data bit 18	SYS_DATA18
27	h_DSS_DAT15	O	OMAP4 LCD pixel data bit 15	SYS_DATA15
28	h_DSS_DAT16	O	OMAP4 LCD pixel data bit 16	SYS_DATA16
29	h_DSS_DAT7	O	OMAP4 LCD pixel data bit 7	SYS_DATA7
30	h_DSS_DAT13	O	OMAP4 LCD pixel data bit 13	SYS_DATA13
31	h_DSS_DAT8	O	OMAP4 LCD pixel data bit 8	SYS_DATA8
32	NC		No Connect	NC
33	h_DSS_DAT9	O	OMAP4 LCD pixel data bit 9	SYS_DATA9
34	h_I2C2_SCL	O	OMAP4 I2C2 serial clock	SYS_I2C1_SCL
35	h_DSS_DAT6	O	OMAP4 LCD pixel data bit 6	SYS_DATA6
36	h_DSS_PCLK	O	OMAP4 LCD pixel clock	SYS_PCLK
37	h_DSS_DEN	O	OMAP4 LCD pixel data enable	SYS_DATA_EN
38	h_DSS_HSYN	O	OMAP4 LCD horizontal sync	SYS_HSYNC

	C			
39	DGND	GND	Ground bus	GND
40	DGND	GND	Ground bus	GND

Pin	ELC4460 J33			PRO4500J33
	I/O	Signal	Description	
1	VIO_1V8	PWR	ELC4460 1.8 V system I/O voltage	EXT_1V8
2	DCIN_JACK	PWR	5 V supplied from PRO4500	PP5P0V
3	DGND	GND	Ground	GND
4	DGND	GND	Ground	GND
5	DGND	GND	Ground	GND
6	DGND	GND	Ground	GND
7	NC		No Connect	P12V_SUPPLY
8	NC		No Connect	P12V_SUPPLY
9	NC		No Connect	P12V_SUPPLY
10	NC		No Connect	P12V_SUPPLY
11	NC		No Connect	P12V_SUPPLY
12	NC		No Connect	P12V_SUPPLY
13	H_MCSPI1_CS1	O	OMAP4 SPI1 chip select 1 (also UART1_RX)	SYS_TRIG_IN_1
14	H_MCSPI1_SIMO	I/O	OMAP4 SPI1 slave in master out	SYS_TRIG_IN_2
15	H_MCSPI1_SCLK	I/O	OMAP4 SPI1 clock out	DRV_INIT_DONE
16	H_MCSPI1_CS0	O	OMAP4 SPI1 chip select 0	DRV_TRIG_OUTB_2
17	H_MCSPI1_CS2	O	OMAP4 SPI1 chip select 2 (also UART1_CTS)	DRV_EXT_POWER_ON
18	H_MCSPI1_SOMI	I/O	OMAP4 SPI1 slave out master I	DRV_TRIG_OUTB_1
19	DGND	GND	Ground bus	GND
20	DGND	GND	Ground bus	GND
21	USBH3_DM	I/O	OMAP4 USB host port 3 data minus	SYS_USB_DN
22	DGND	PWR	Ground bus	GND
23	USBH3_DP	I/O	OMAP4 USB host port 3 data plus	SYS_USB_DP
24	H_GPMC_AD13	I/O	OMAP4 GPMC address or data bit 13	DRV_GPIO12
25	DGND	GND	Ground bus	GND
26	H_MCSPI1_CS3	O	OMAP4 SPI1 Chip Select 3 (also UART1_RTS)	SYS_MSTR_MUX_SEL
27	H_GPMC_AD14	I/O	OMAP4 GPMC address or data bit 14	DRV_GPIO11
28	h_DMTIMER11_PWM	O	OMAP4 display PWM control	SYS_GPIO5
29	DGND	GND	Ground bus	GND
30	H_GPMC_AD15	I/O	OMAP4 GPMC address or data bit 15	SYS_USB_SEL
31	H_GPMC_AD12	I/O	OMAP4 GPMC address or data bit 12	SYS_GPIO6
32	H_GPMC_AD8	I/O	OMAP4 GPMC address or data bit 8	DRV_GPIO00
33	H_GPMC_WAIT0	I	OMAP4 GPMC Wait input 0	SYS_TRIGGER_SEL
34	H_GPMC_AD9	I/O	OMAP4 GPMC address or data bit 9	SYS_UART_SEL
35	H_UART4_TX	O	OMAP4 UART4 transmit data	SYS_UART0_RXD

36	H_UART4_RX	O	OMAP4 UART4 receive data	DRV_UART0_TXD
37	H_GPMC_NCS0	O	OMAP4 LCD pixel data enable	DRV_TRIG_OUTA_2
38	H_GPMC_AD10	I/O	OMAP4 GPMC address or data bit 10	DRV_GPIO02
39	H_GPMC_NCS1	O	OMAP4 GPMC Chip Select 0	SYS_I2C_OE
40	H_GPMC_AD11	I/O	OMAP4 GPMC address or data bit 11	DRV_TRIG_OUTA_1

To configure the OMAP4 LCD peripheral drive for the PRO4500 24-bit RGB input, perform the following changes to the boot script. The boot script, boot.scr, is used by U-Boot.

• Set the DVI as the default output by adding the following entry to boot.scr:

– omapfb.mode=dvi omapdss.def_disp=dvi

• Set the desired resolution fro the PRO4500 output by adding one of the following entries to boot.scr:

– omapfb.mode=dvi:912x1140MR-24@60

– omapfb.mode=dvi:1280x800MR-24@60

• Generate the boot.scr:

– mkimage -A arm -T script -C none -n "Boot Image" -d boot.script boot.scr

• Copy the generated uImage and boot.scr in the boot partition of the SD card.

Make the modules:

• Make CROSS_COMPILE = arm-linux-gnueabi-ARCH = arm INSTALL_MOD_PATH = <path_of_modules> modules_install

Copy the ‘modules’ folder from the path given in the previous command to the folder on secondary partition.

Chapter 7 Connectors

This chapter describes the connector pins of the PRO4500 module.

7.1 Input Trigger Connectors

Table 7-1 lists the input trigger connector (J11) pins. The trigger inputs have hysteresis. Two matching six-pin, 1.25-mm connector part numbers are:

- Molex part number: 51021-0600
- Digi-Key part number: WM1724-ND

The corresponding connector terminal (crimp) part numbers are:

- Molex part number: 50079-8100
- Digi-Key part number: WM2023-ND

Table 7-1. Input Trigger Connector Pins

Description	Pin	Supply Range
Trigger In 1 supply	1	External or internal 1.8-V and 3.3-Velectable at J10
Trigger In 1	2	
Ground	3	Ground
Trigger In 2 supply	4	External or internal 1.8-V and 3.3-Velectable at J12
Trigger In 2	5	
Ground	6	Ground

7.2 Output Trigger Connectors

Table 7-2 lists the output trigger connector (J14) pins. Two matching six-pin, 1.25-mm connector part numbers are:

- Molex part number: 51021-0600
- Digi-Key part number: WM1724-ND

The corresponding connector terminal (crimp) part numbers are:

- Molex part number: 50079-8100
- Digi-Key part number: WM2023-ND

Table 7-2. Output Trigger Connector Pins

Description	Pin	Supply Range
Trigger Out 1 supply	1	External or internal 1.8-V and 3.3-Velectable at J13
Trigger Out 1	2	
Ground	3	Ground
Trigger Out 2 supply	4	External or internal 1.8-V and 3.3-Velectable at J15
Trigger Out 2	5	
Ground	6	Ground

7.3 DLPC350 UART

The DLPC350 UART compatible cable:

- Leopard Imaging: LI-SER-01
- Mouser part number: 931-LI-SER-01

Table 7-3 lists UART connector (J20) pins.

Table 7-3. UART Connector Pins

Description	Pin	Supply Range
Ground	1	0V
RX	2	3.3 V
TX	3	3.3 V

7.4 DLPC350 I2C0

Table 7-4 lists the I2C0 connector (J16) pins. Two matching four-pin, 1.25-mm connector part numbers are:

- Molex part number: 51021-0400
- Digi-Key part number: WM1722-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 50079-8100
- Digi-Key part number: WM2023-ND

Table 7-4. I 2 C0 Connector Pins

Description	Pin	Supply Range
I 2 C SCL	1	3.3 V
I2 C SDA	2	3.3 V
3.3-V supply	3	3.3 V
Ground	4	0V

7.5 DLPC350 I2C1

Table 7-5 lists the I2C1 connector (J17) pins. Two matching four-pin, 1.25-mm connector part numbers are:

- Molex part number: 51021-0400
- Digi-Key part number: WM1722-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 50079-8100
- Digi-Key part number: WM2023-ND

Table 7-5. I 2C1 Connector Pins

Description	Pin	Supply Range
I 2C SCL	1	3.3 V
I2C SDA	2	3.3 V
3.3-V supply	3	3.3 V
Ground	4	0V

7.6 Fan

Table 7-6 lists the fan connector (J22) pins. Two matching three-pin, 1.25-mm connector part numbers are:

- Molex part number: 51021-0300
- Digi-Key part number: WM1722-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 50079-8100
- Digi-Key part number: WM2023-ND

Table 7-6. Fan Connector Pins

Description	Supply	Range
Power	**1**	12 V
FAN_LOCKED	**2**	3.3 V
Ground	**3**	0V

7.7 LED Control

Table 7-7 lists the red LED connector (J31) pins. Two matching nine-pin, 1.5-mm connector part numbers are:

- Molex part number: 87439-0900
- Digi-Key part number: WM2093-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 87421-0000
- Digi-Key part number: WM1112-ND

Table 7-7. LED Control Connector Pins

Description	Supply	Range
BLU_LED_EN	1	3.3 V
LEDB_PWM	2	3.3 V
Ground	3	0V
GRN_LED_EN	4	3.3 V
LEDG_PWM	5	3.3 V
Ground	6	0V

RED_LED_EN	7	3.3 V
LEDR_PWM	8	3.3 V
Ground	9	0V

7.8 LED Power

Table 7-8 lists the green LED connector (J5) pins. Two matching six-pin, 1.5-mm connector part numbers are:

- Molex part number: 87439-0900
- Digi-Key part number: WM2093-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 87421-0000
- Digi-Key part number: WM1112-ND

Table 7-8. LED Power Connector Pins

Description	Supply	Range
P3P3V	1	3.3 V
SCL0	2	3.3 V
SDA0	3	3.3 V
P12V_CONN	4	12 V
P12V_CONN	5	12 V
P12V_CONN	6	12 V
Ground	7	0V
Ground	8	0V
Ground	9	0V

7.9 FPD-Link

Table 7-9 lists the FPD-Link connector (J9) pins. The 20-pin, 0.5 SMT header is:

- Panasonic part number: AXK6S20647YG

Table 7-9. FPD-Link Connector Pins

Description	Supply	Range
RCK_IN_P	1	1.2 V
RXE_AP	2	1.2 V
Ground	3	0 V
Ground	4	0 V
RCK_IN_N	5	1.2 V
RXE_AN	6	1.2 V
RXE_BP	7	1.2 V
RXE_CP	8	1.2 V
Ground	9	0 V
Ground	10	0 V
RXE_BN	11	1.2 V

RXE_CN	12	1.2 V
RXE_DP	13	1.2 V
RXE_EP	14	1.2 V
Ground	15	0 V
Ground	16	0 V
RXE_DN	17	1.2 V
RXE_EN	18	1.2 V
NC	19	N/A
NC	20	N/A

7.10 JTAG Boundary Scan

Table 7-10 lists the JTAG boundary connector (J25) pins. Two matching six-pin, 1.25-mm connector part numbers are:

- Molex part number: 51021-0600
- Digi-Key part number: WM1724-ND

The corresponding connector terminal (crimp) part numbers are:

- Molex part number: 50079-8100
- Digi-Key part number: WM2023-ND

Table 7-10. JTAG Boundary Scan Connector Pins

Description	Supply	Range
TRST	1	3.3 V
TDI	2	3.3 V
TMS1	3	3.3 V
TDO1	4	3.3 V
TCK	5	3.3 V
Ground	6	0 V

7.11 Power

Table 7-11 lists the power socket (J26) pins. Two matching connector part numbers are:

- Switchcraft part number: 760
- Digi-Key part number: SC1051-ND

Table 7-11. Power Connector Pins

Description	Supply	Range
Input supply	1	12 V
Ground	2	0V
Ground	3	0V

Appendix A Safety

WARNING

Possible hazardous optical radiation emitted from this product. Do not stare at operating LEDs. May be harmful to eyes. Also, avoid touching components during operation.

CAUTION

To minimize the risk of fire or equipment damage, make sure that air is allowed to circulate freely around the PRO4500 board when operating.

CAUTION

The kit contains ESD-sensitive components. Handle with care to prevent permanent damage.